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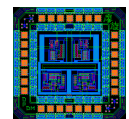
Modern DSP Processors: Architectures and Trends

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DSP/IC
DESIGN LAB

Outline of This Talk

- Introduction
- Applications and Markets
- DSP Processor Fundamentals
- Today's DSP Landscape
- Low Power Enhanced DSP
- High Performance DSP
- Design Example -- CDSP
- Future Trends

DSP v.s. DSP !?

- Digital Signal Processing:
 - Mathematical manipulation of digitally represented signals
- Digital Signal Processor:
 - Microprocessors designed to perform Digital Signal Processing
 - Also called *DSP Processor* or *Programmable DSP (PDSP)*

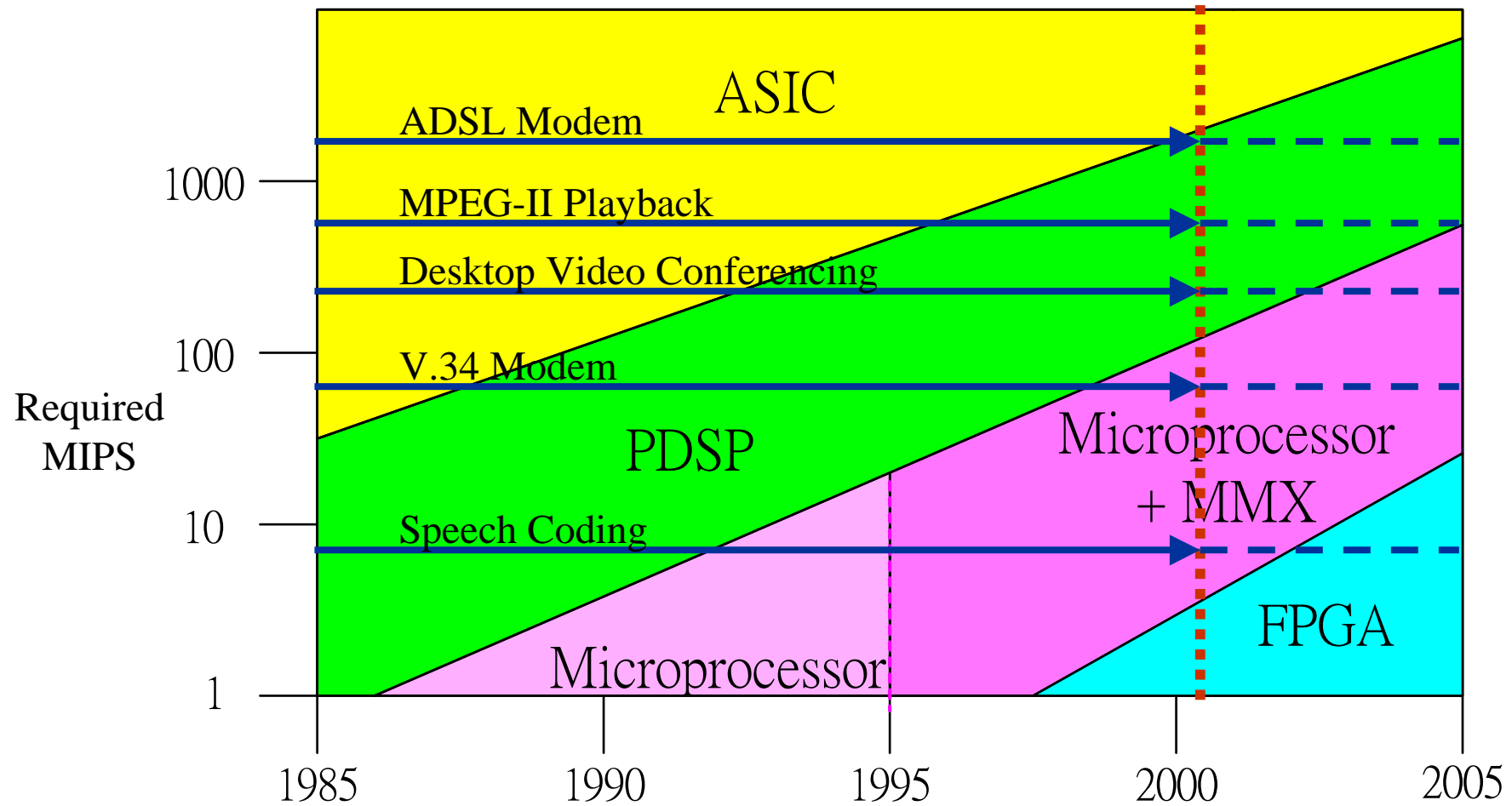
Why Use DSP Processor ?

- DSP Processors have transformed digital signal processing from academic study into viable commercial business for **consumer products**
 - Real-time performance
 - Short time-to-market
 - Upgradable solutions
- Move *Hardware Design* to *Software Design*
(ASIC) (Programming)
- Offer the key to **SOC** integration

Applications and Markets

- Video Game Consoles
- Handheld, Palmtop, Automobile, and Network PCs
- Answer Machines
- Digital Hearing Aids
- Set-Top Boxes and DVD
- Digital Cameras
- MP3 Players
- ADSL/HDSL
- Radio Decoders
- Video Phones
- Cellular Phones
- Cable Modem
- Modems, Fax Machines
- Cordless Phones
- Voice over IP

DSP Hits the Mainstream !



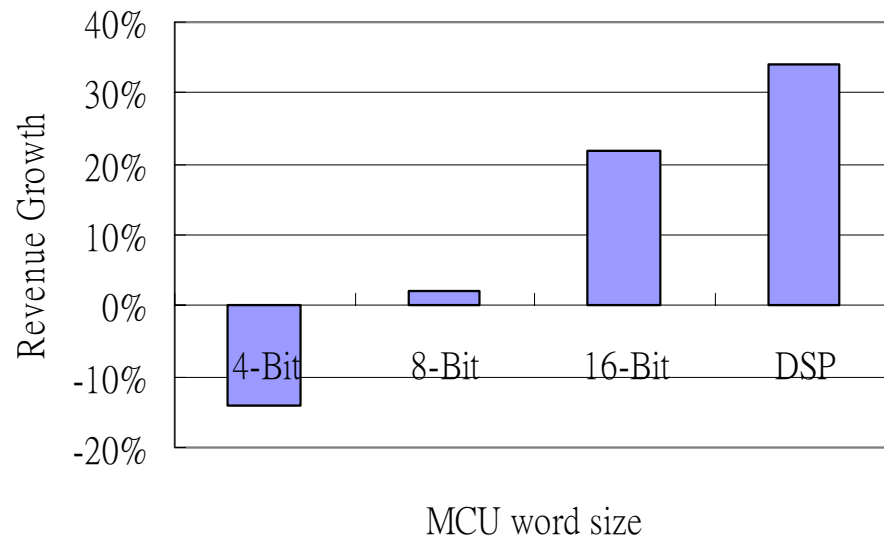
全球 IC 產業規模

年度		1999	2000	2001
市場規模 (億美元)	DRAM	180	250	370
	SRAM	43	48	53
	快閃記憶體	41	55	66
	微處理器	280	320	400
	微控制器	140	180	220
	類比IC	210	250	300
	分離式元件	130	150	160
	其他	416	487	521
	全體IC	1,440	1,740	2,090
	佔有率 (%)	DRAM	12.5	14.4
SRAM		2.9	2.8	2.5
快閃記憶體		2.8	3.2	3.2
微處理器		19.4	18.4	19.1
微控制器		9.7	10.3	10.5
類比IC		14.6	14.4	14.4
分離式元件		9.0	8.6	7.7
其他		28.9	28.0	24.9
全體IC		100	100	100

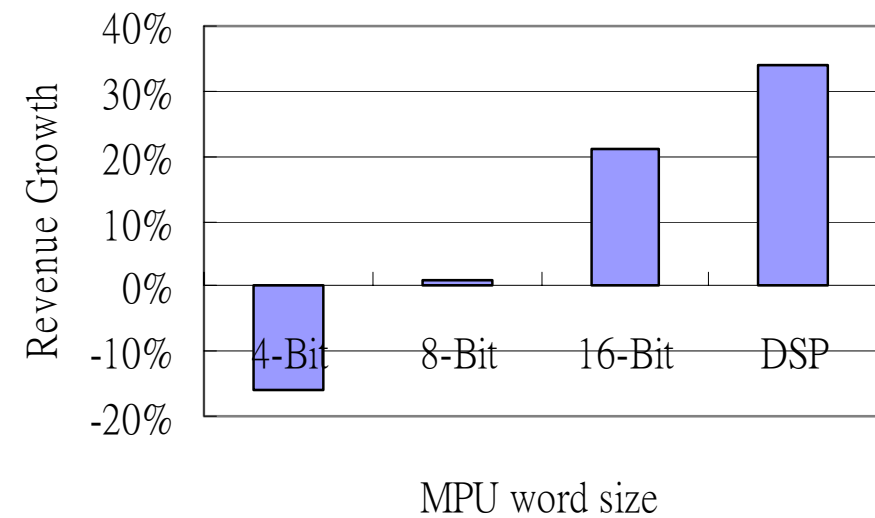
資料來源：SIA，1999年10月（預估值）

Market Growth

Five-Year MCU Market Growth versus DSP

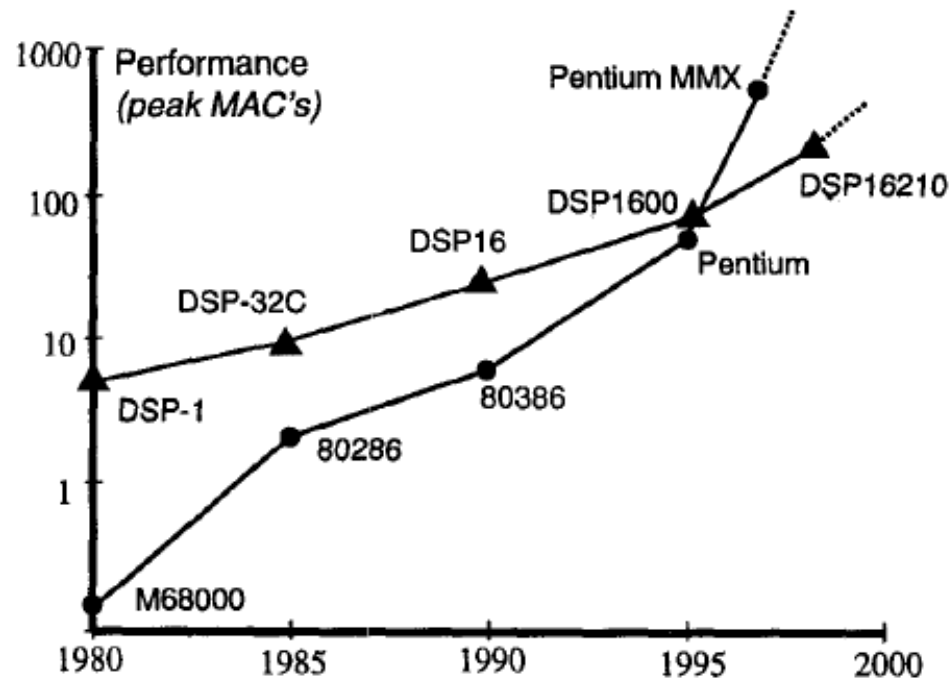


Five-Year MPU Market Growth versus DSP

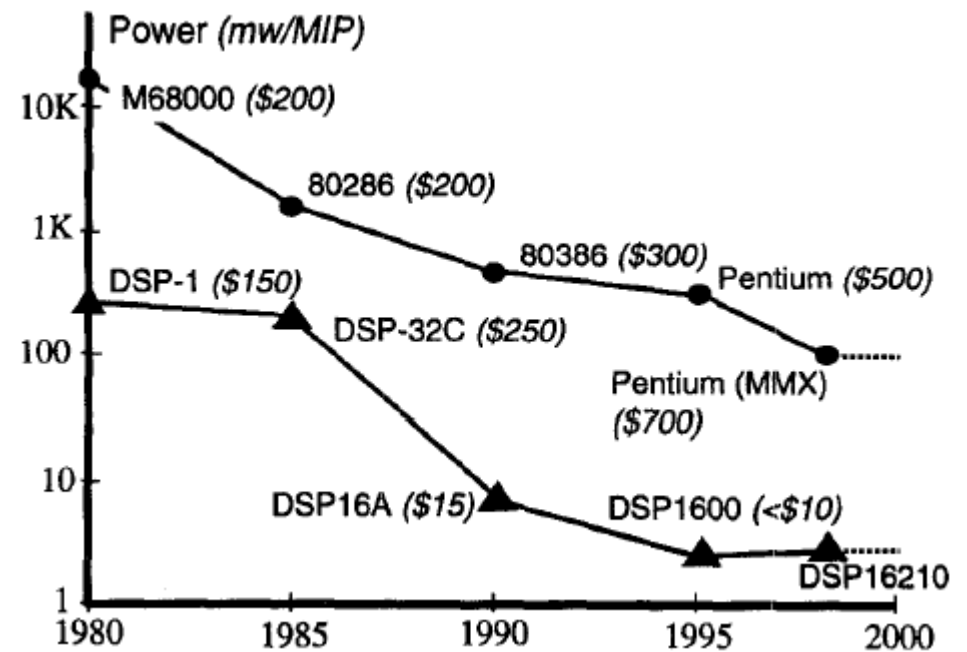


DSP v.s. MPU

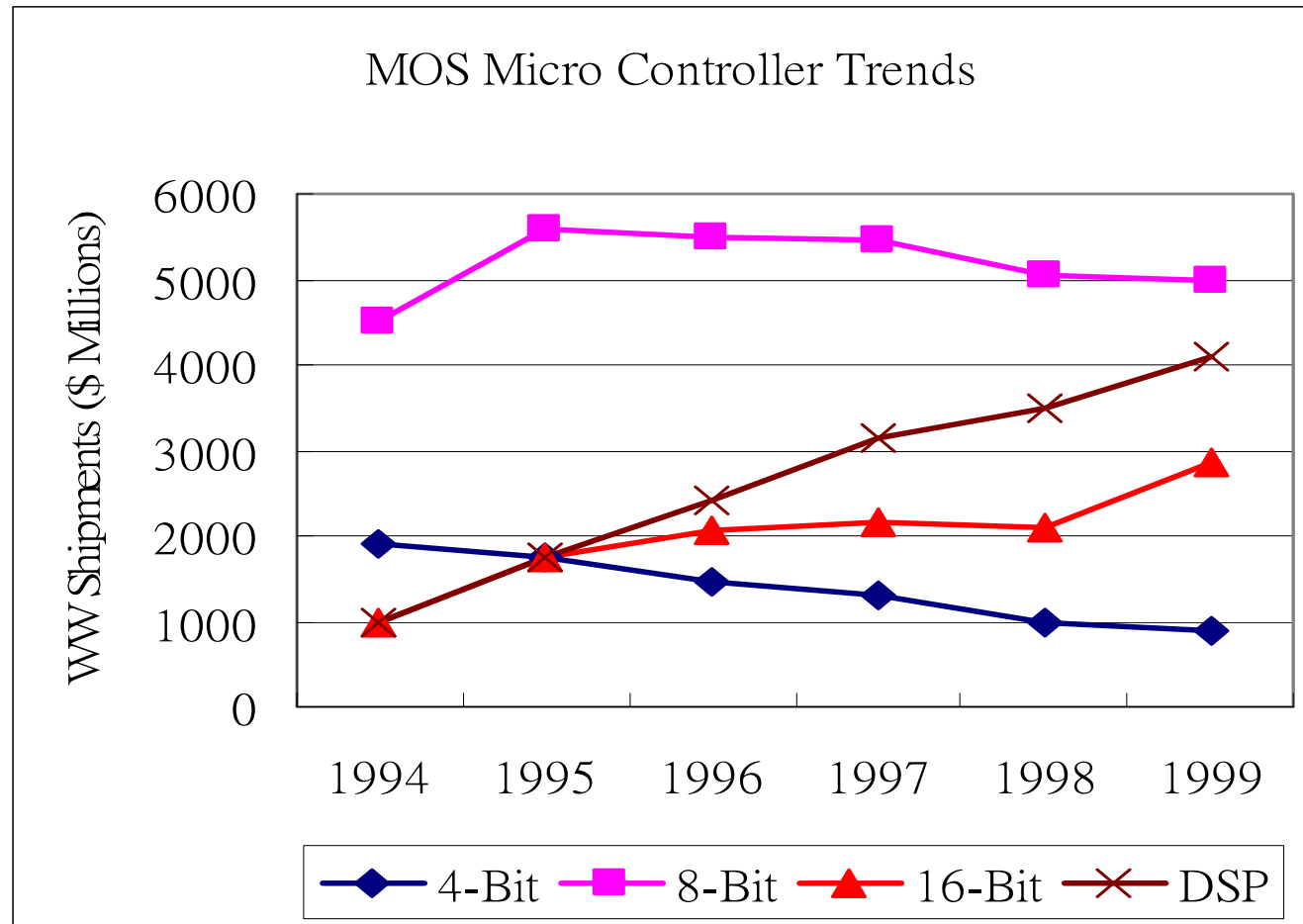
Performance



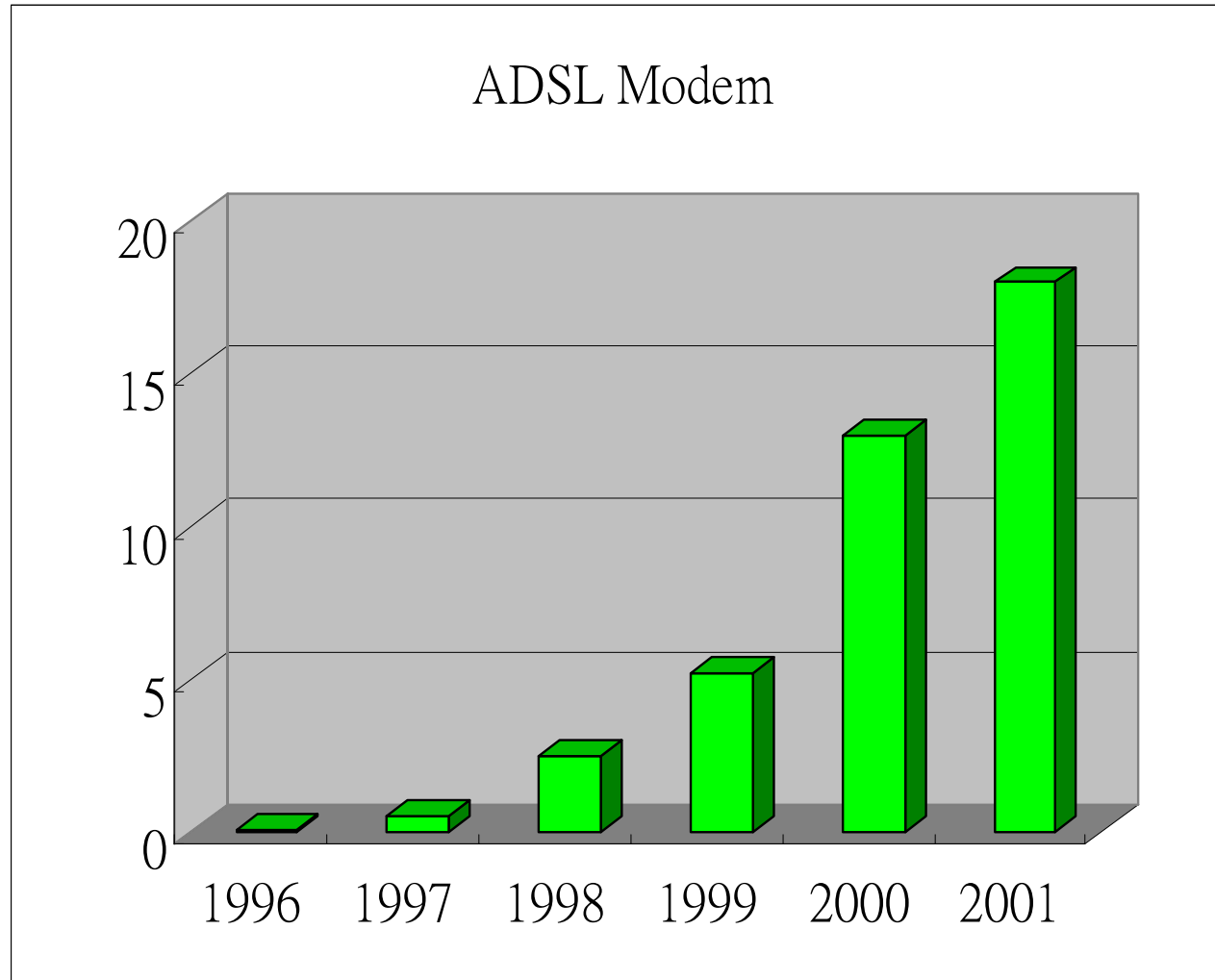
Power and Cost



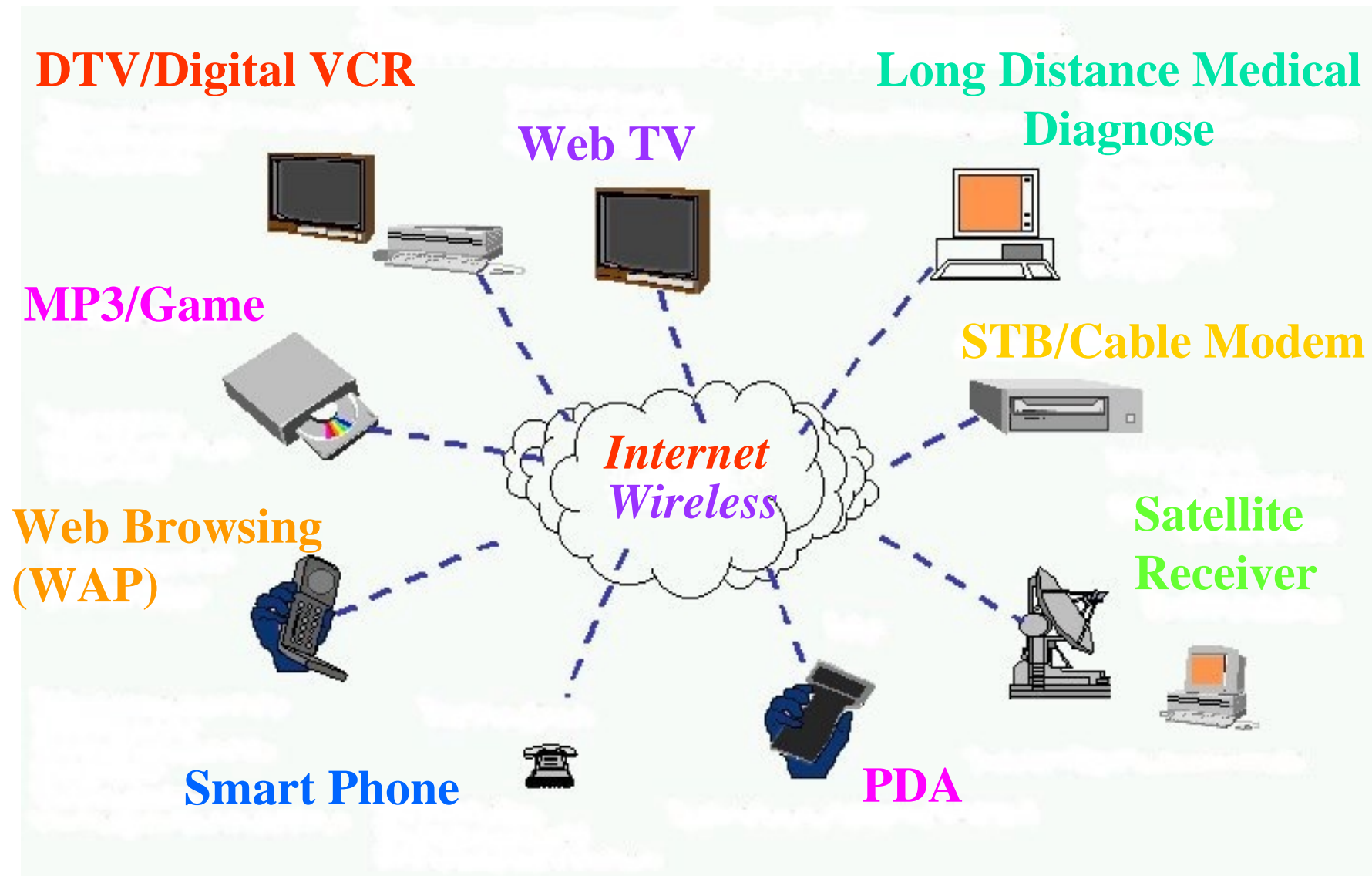
DSP Outpaces MCU Markets



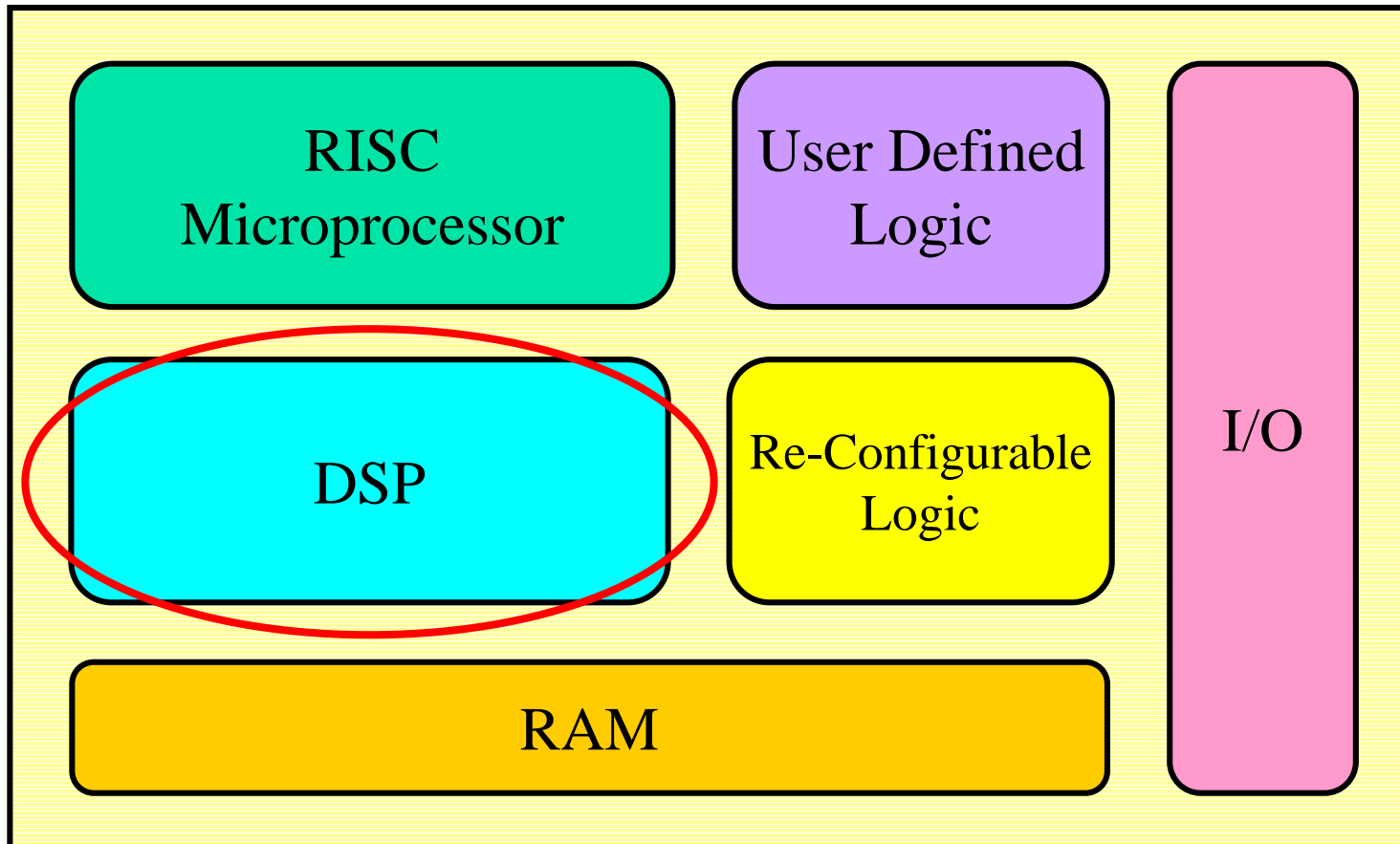
ADSL Modem Market Growth



Information Appliance



SOC Integration



DSP Processor Characteristic

- Fast Multiplication
 - For inner product computation of many DSP algorithms
 - Single cycle multiply-accumulate (MAC)
- Multiple Data Processing Units
 - Separate MAC, ALU, Comparator (CMP), and Barrel Shifter (SFT)
- Multiple Memory Access Architecture
 - One program fetch and multiple data R/W in each instruction cycle
 - Harvard memory architecture

DSP Processor Characteristic

- Specialized Program Control
 - Zero-overhead looping for repetitive DSP algorithms
- Specialized Addressing Mode
 - Register indirect addressing with post-increment
 - Bit-reversal addressing for FFT
 - Modulo addressing for hardware circular buffers
- Specialized Instruction Sets
 - Speed up specific applications
- On-Chip Peripherals and I/O Interfaces

Data Format

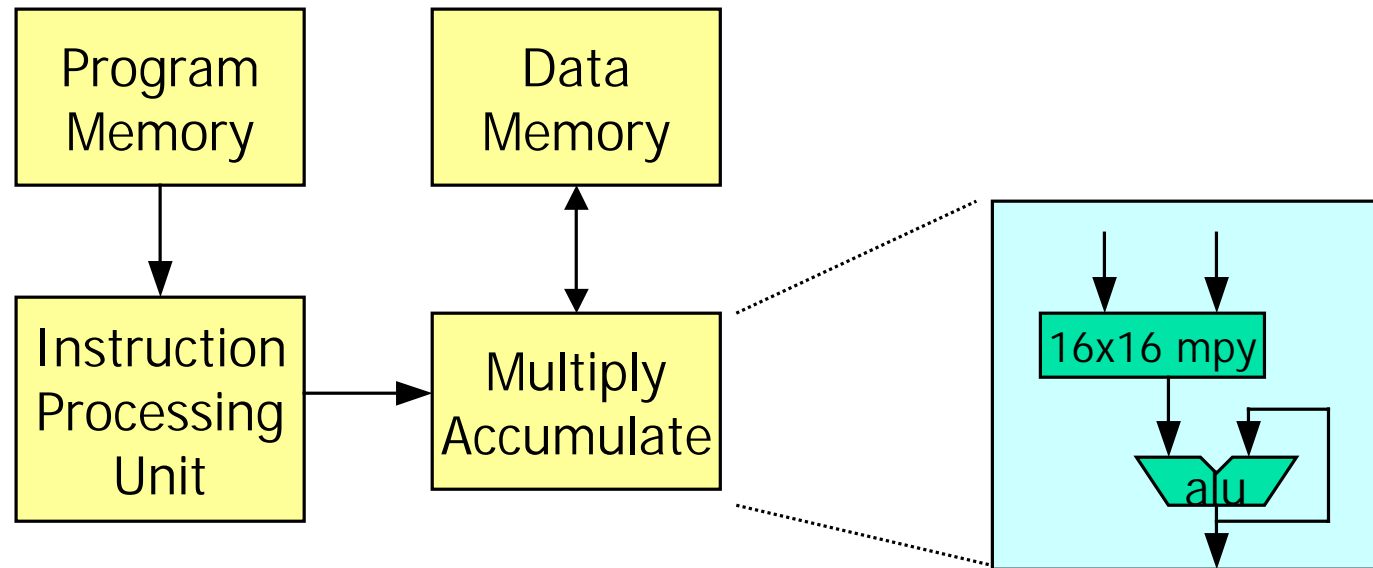
- Arithmetic Format
 - Fixed-point arithmetic
 - Floating-point arithmetic
- Data Width
 - Fixed-point data
 - 16-bit, 20-bit, or 24-bit
 - Trade-off between applications and cost
 - Floating-point data
 - 32-bit

Evolution of DSP Processors

Generation	Features	Examples
0 (1980)	Von Neumann architecture	DSP-1 (AT&T)
1 (1982)	Basic Harvard architecture	TMS320C10 (TI) NEC7720
2 (1986)	1 data/program bus, 1 data bus	TMS320C25 (TI) DSP16A (AT&T)
3 (1990)	Extra addressing modes, extra functions	TMS320C5X (TI) DSP16xx (AT&T)
4 (1994)	2 data busses, 1 program bus	TMS320C54X (TI)
5 (1996-now)	2 data busses, 1 program bus, multiple units	Lucent 16xxx Atmel Lode Siemens Carmel

Basic Harvard Architecture

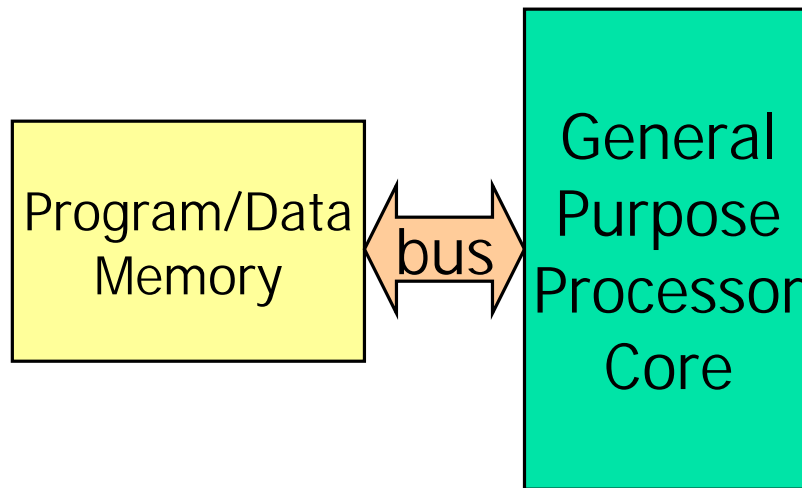
Separate Data Memory from Program Memory



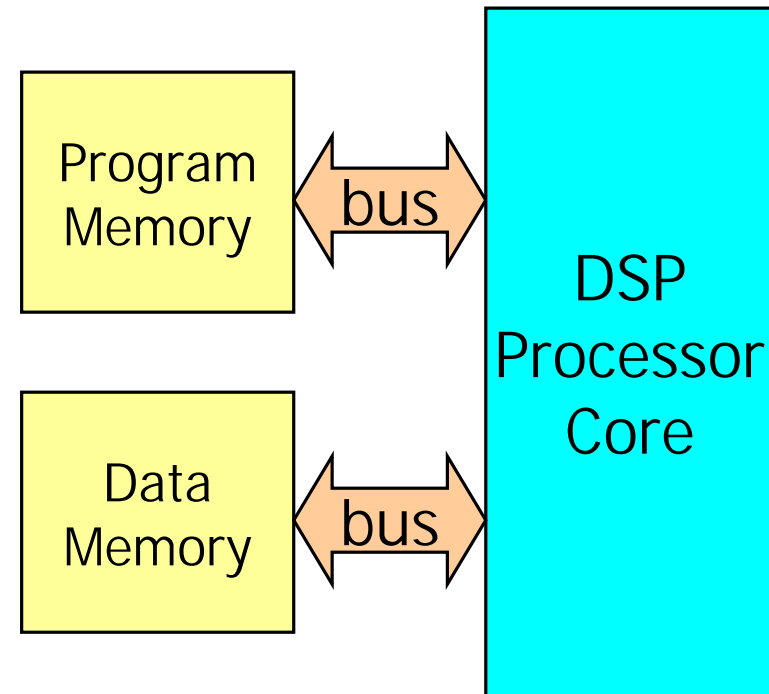
Different from Von Neumann machine:

One address bus – one data bus – one memory space

Differences of DSP and MPU in Memory Architecture



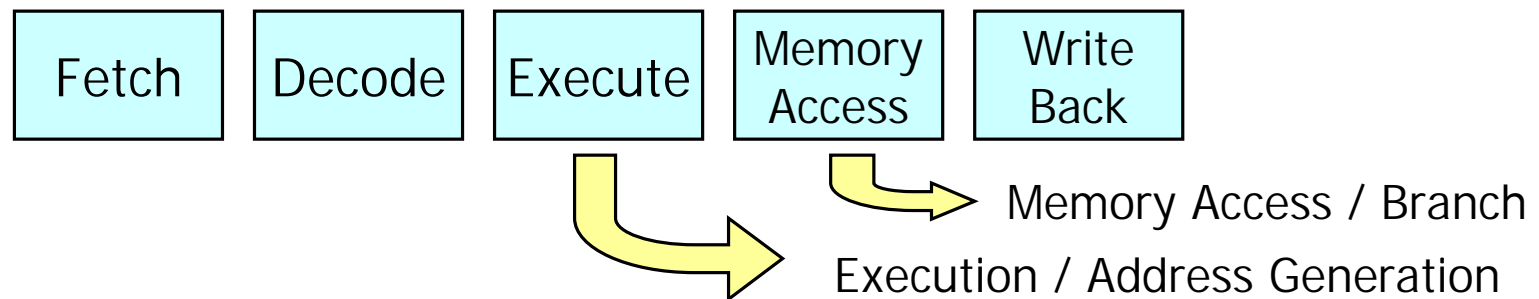
Microprocessor



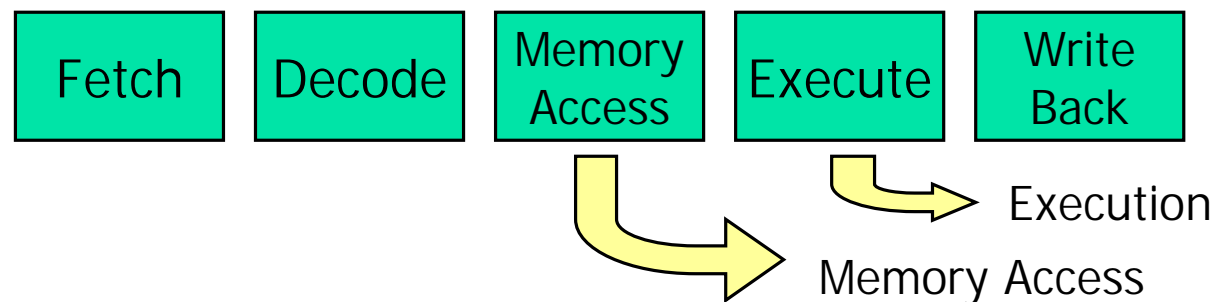
DSP

Control & Pipeline for DSP

RISC



DSP



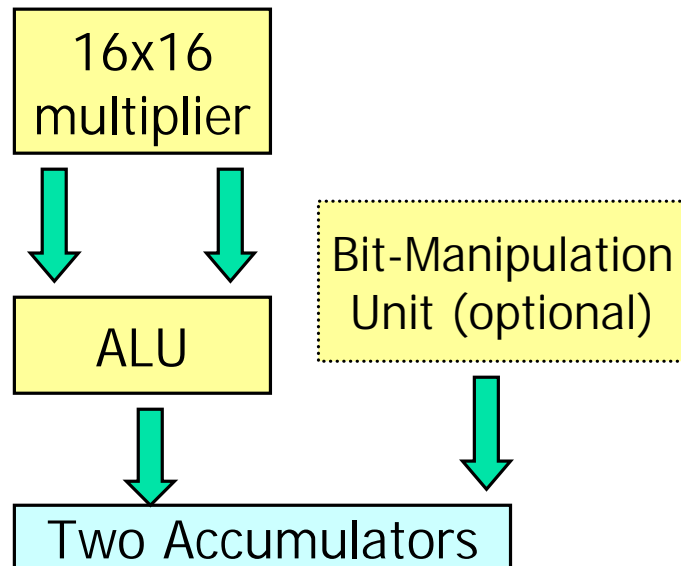
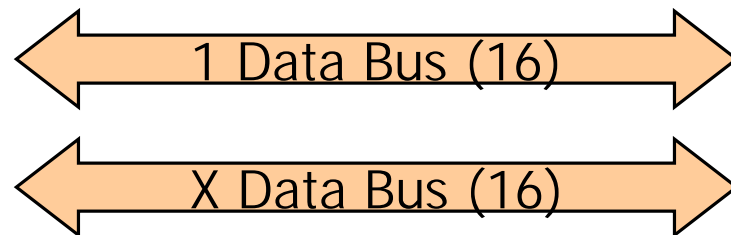
Today's DSP Landscape

- Low-Cost Workhorse (<100 MIPS) :
 - Conventional DSP processor
 - ADI ADSP-21xx, TI C2x, and Motorola DSP560xx
- Low-Power Mid-Range (100 ~ 1000 MIPS) :
 - Enhanced architecture based on conventional DSP
 - Lucent DSP 16xxx, TI C54x and C55x
- Diversified High-End (>1000 MIPS) :
 - Deeper pipeline stage to increased clock rate
 - More parallelism
 - TI C6x and ADI TigerSHARC

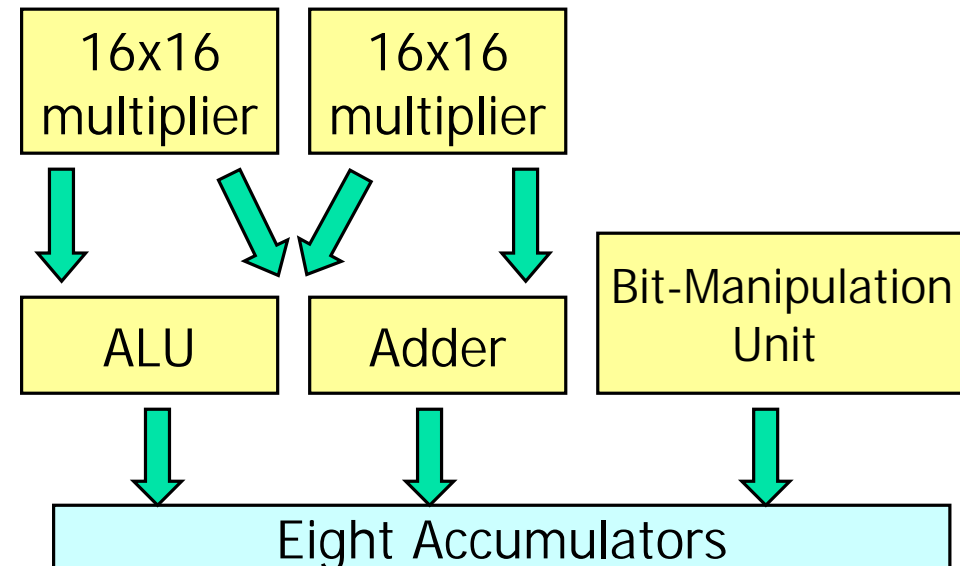
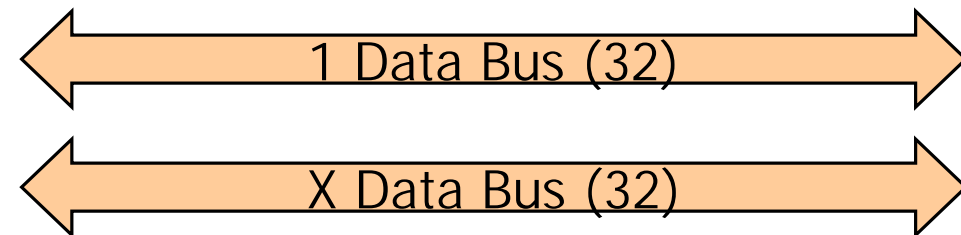
Low-Power Mid-Range DSP

- Enhanced Conventional DSP Processors
 - = > **Domain-Specific DSP Processors**
 - Enhance architecture according to target domain
- High performance
 - Enough performance for target application domain
- Low power
 - Due to reduce required MIPS and thus lower down clock rate
- High degree of programmability
 - Although sacrifice some flexibility

Enhanced Architecture



Conventional DSP Processors



Enhanced Conventional DSP Processors

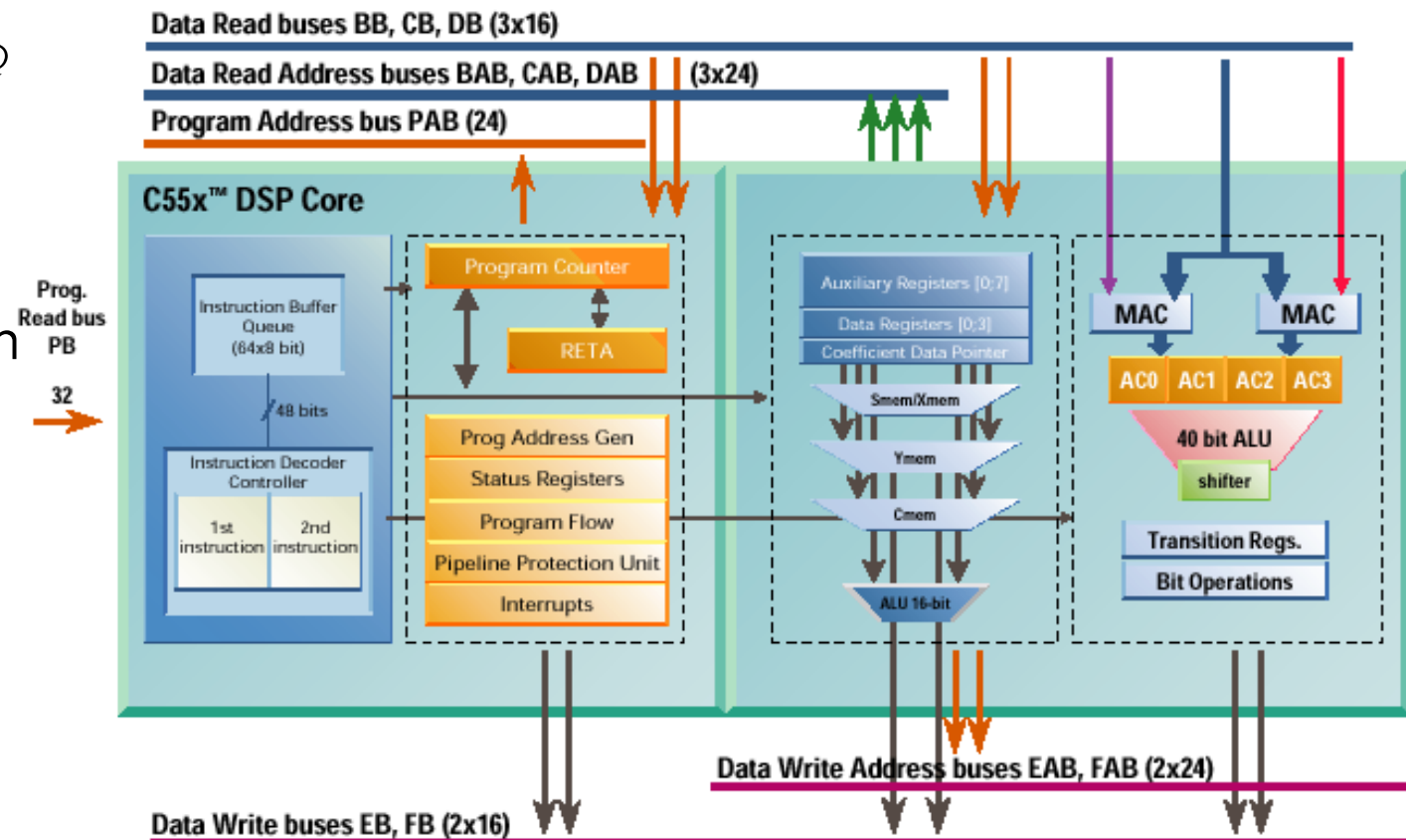
Low Power Strategies

- Power Management
 - Gated clock
 - Power off un-used parts
 - Reduce clock rate of idle parts
- Variable Instruction Length
- Compressed Instruction
- Full-Custom Data Path Layout
- Technology and Voltage Scaling

TI TMS320C55x

Enhanced Architecture

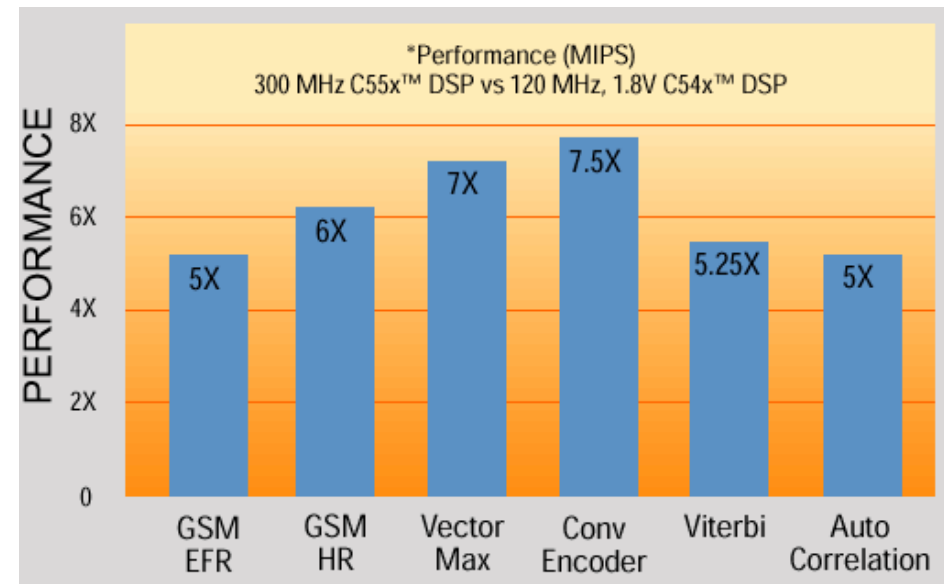
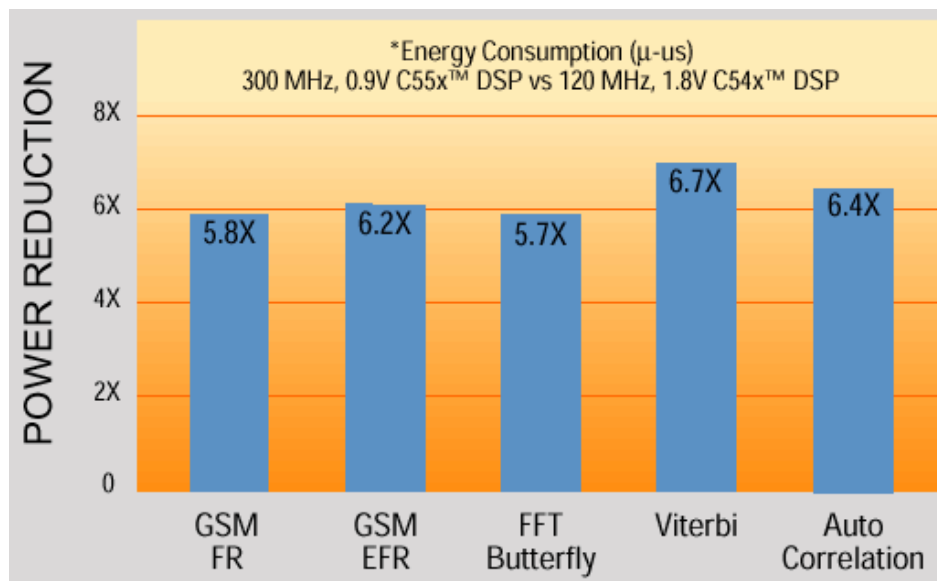
- 0.05mW/MIPS @ 0.9V
- 140-800 MIPS
- Variable instruction length
- 2 MACs, 2 ALUs
- 3 data read bus
- 2 data write bus



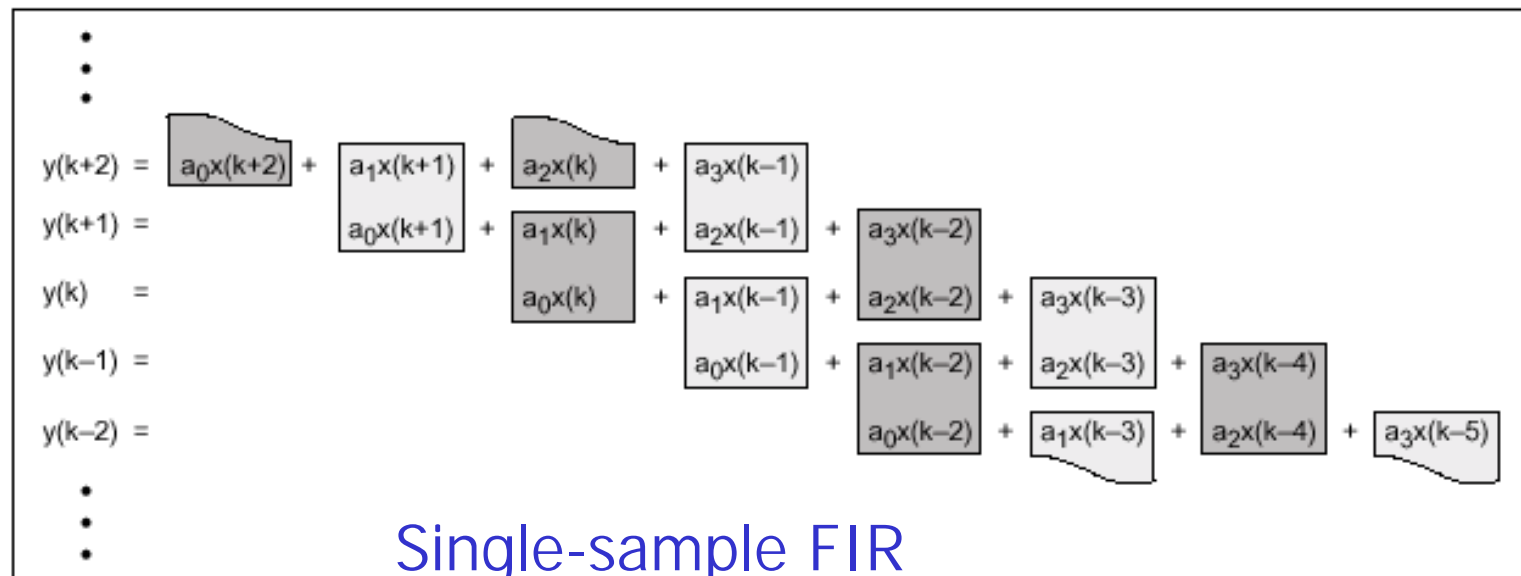
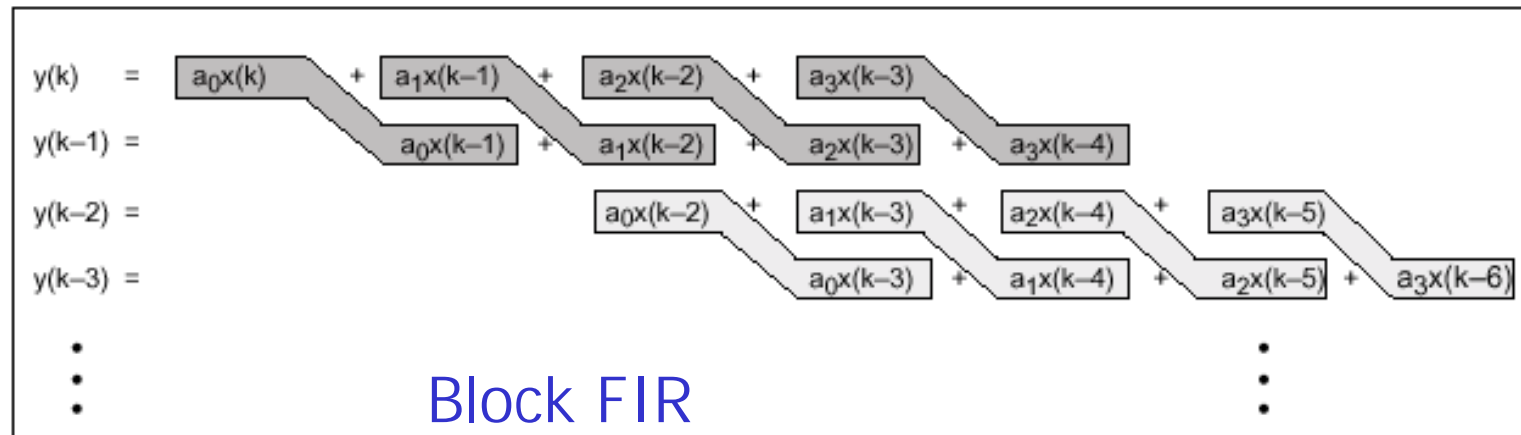
TI TMS320C55x

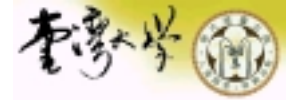
Low Power Strategies

- Automatic Power Management
- Increase Idle Domains
- Variable Instruction Length
- Increase Parallelism



FIR Filtering at TI C55x

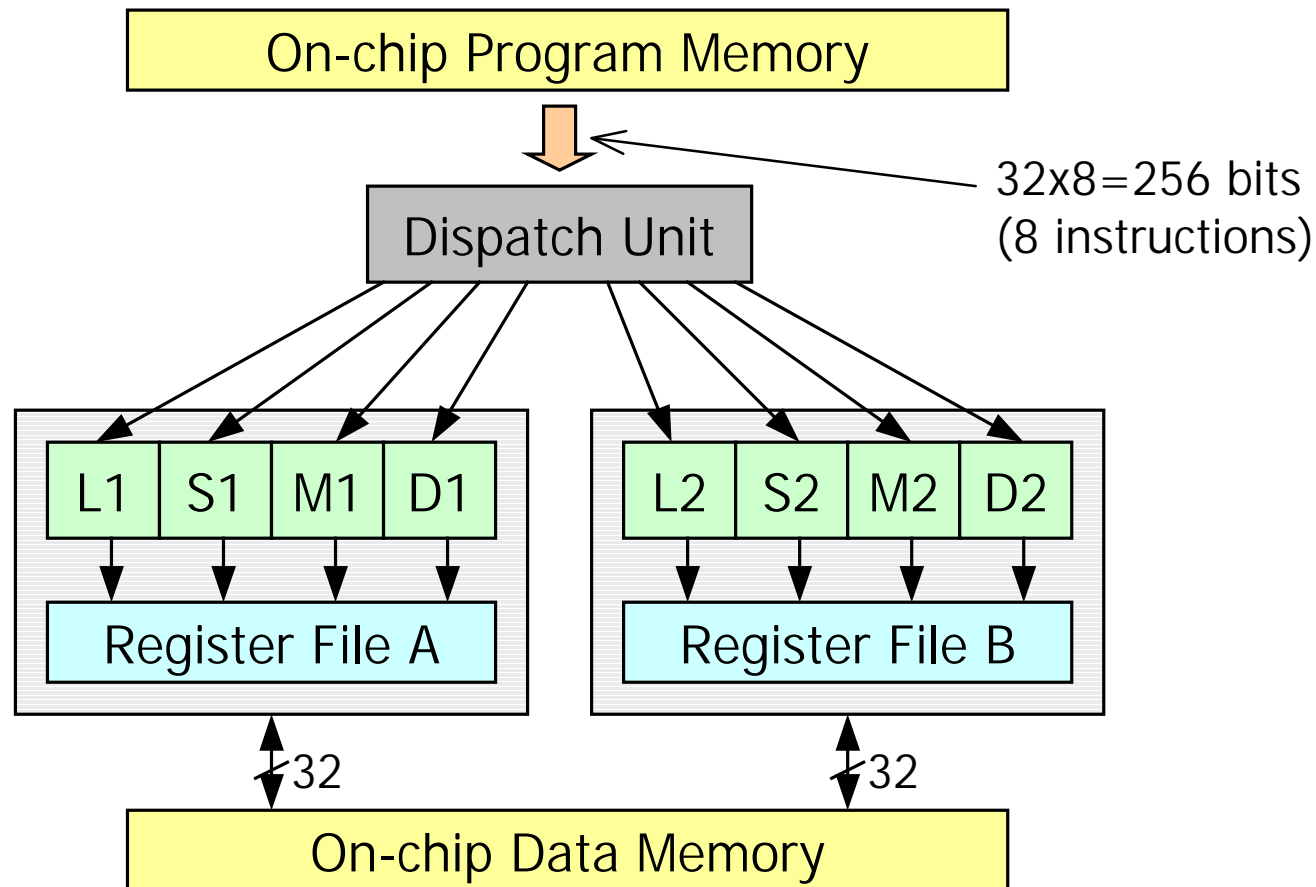




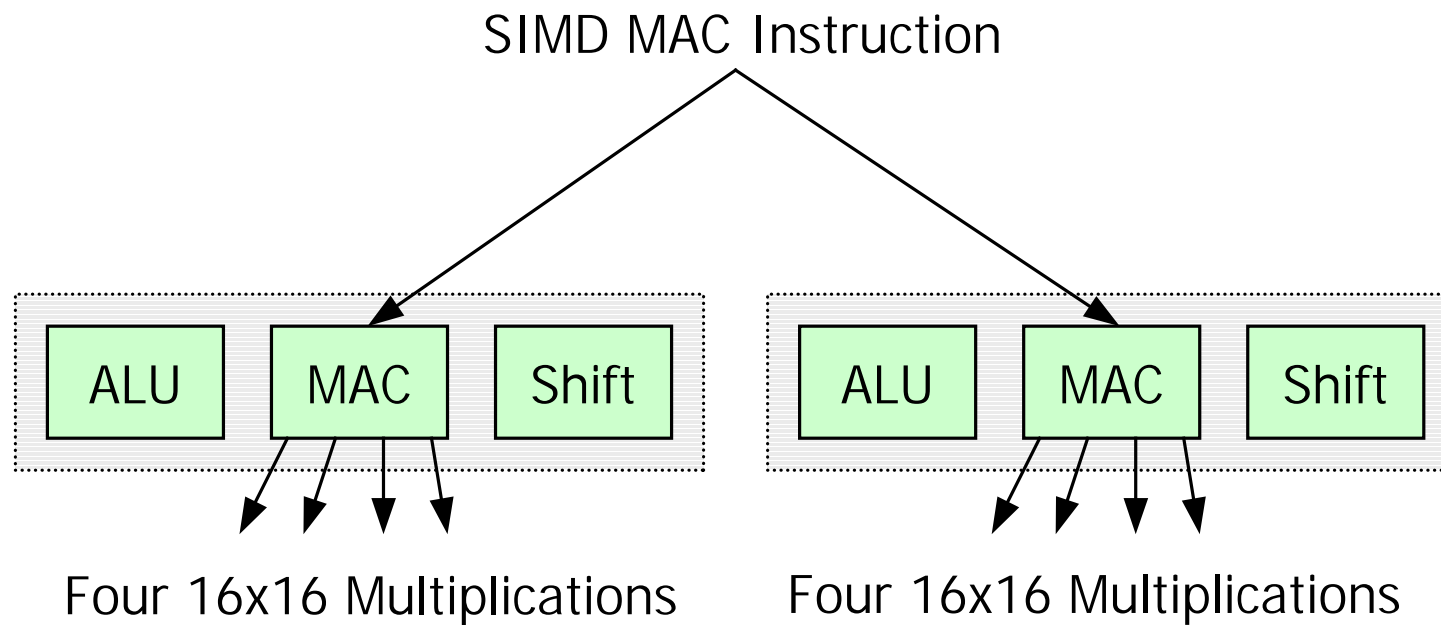
Diversified High-End DSP

- Very deep pipeline for high clock rate
- Domain specific instruction set
- Wider memory bandwidth
- More parallelism
 - Superscalar
 - **VLIW** (Very-Long-Instruction-Word)
 - **SIMD** (Single-Instruction Multiple-Data)
 - **SWP** (Sub-Word Parallel)
 - **MIMD** (Multiple-Instruction Multiple-Data)

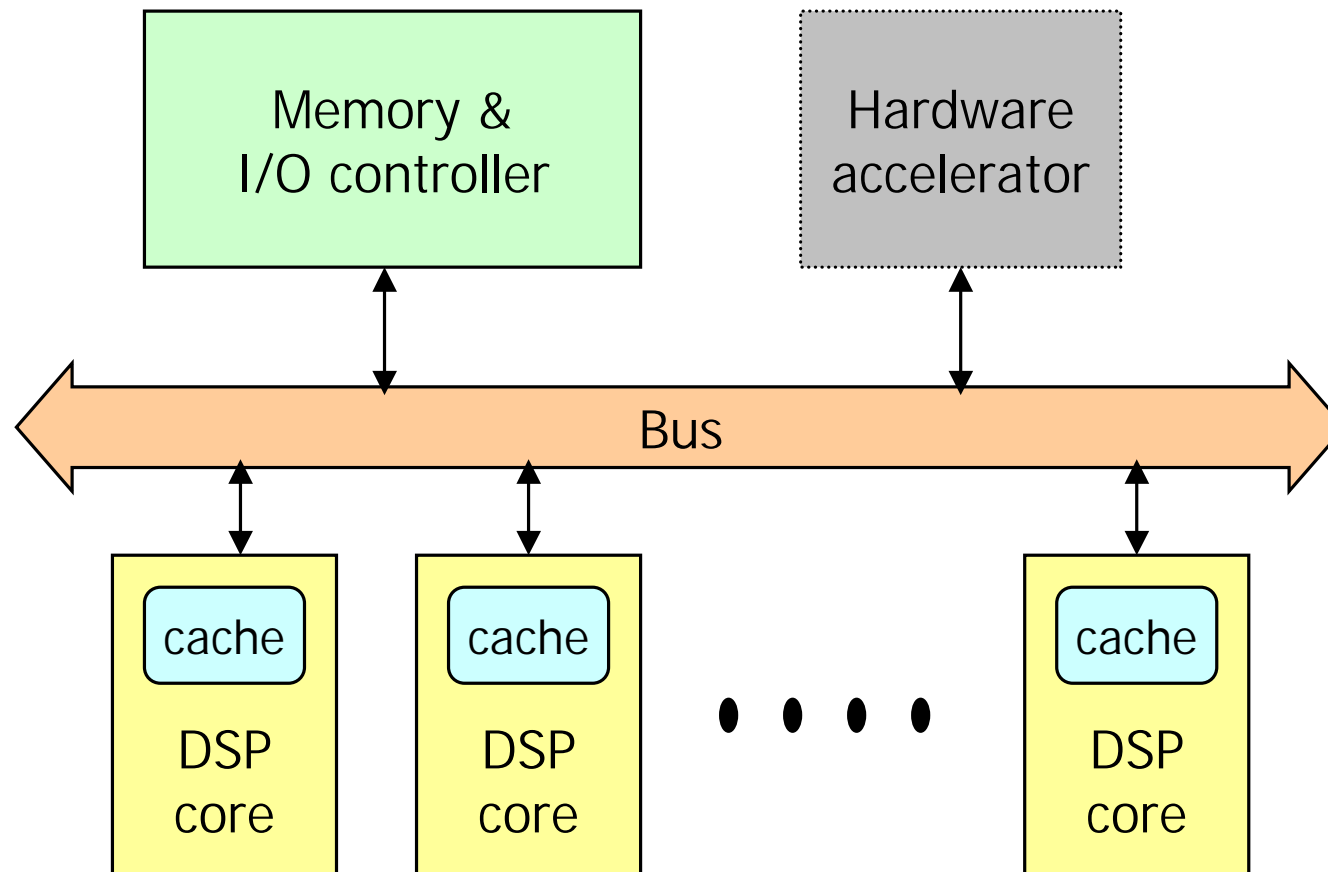
VLIW



SIMD and SWP

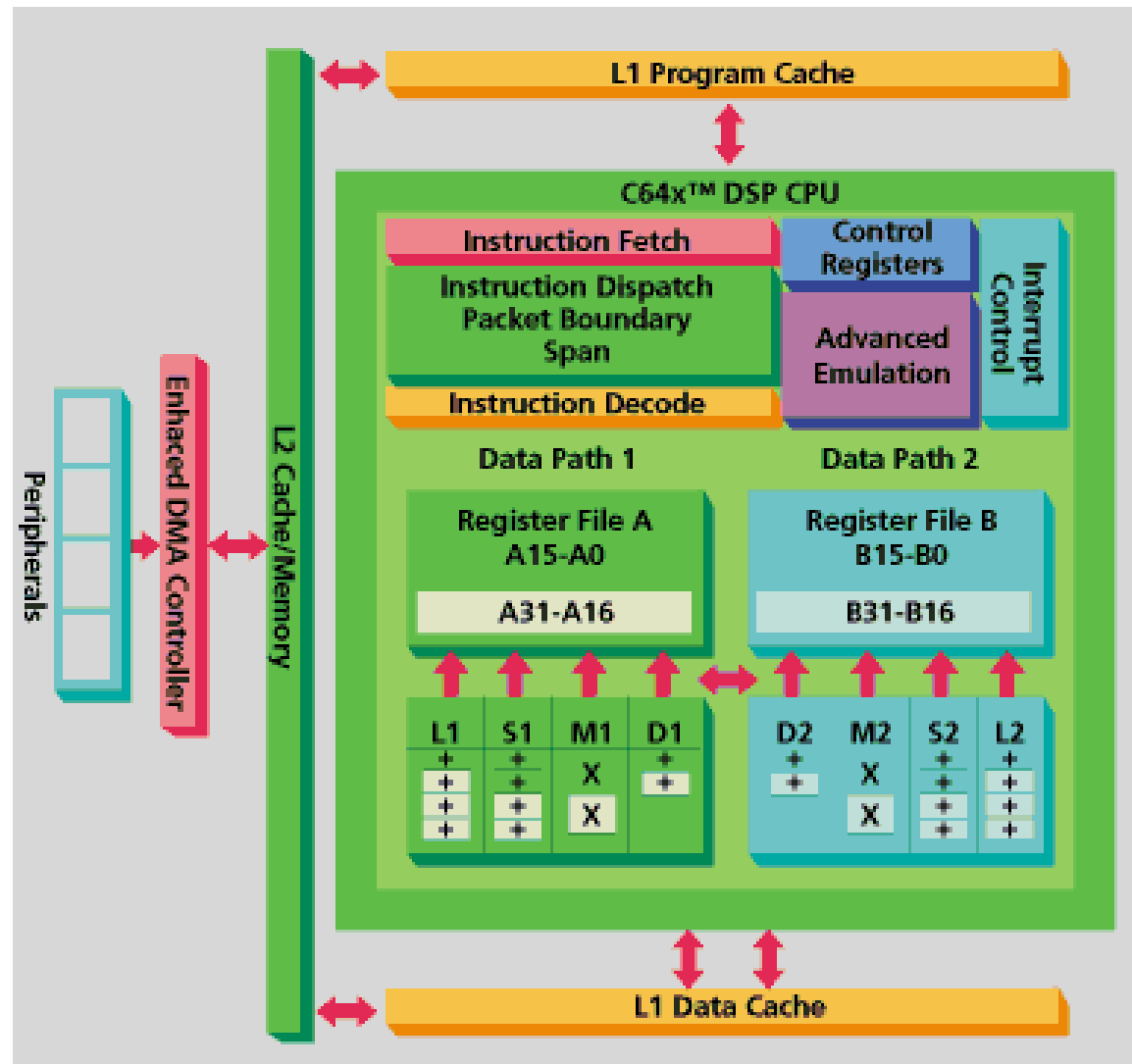


MIMD



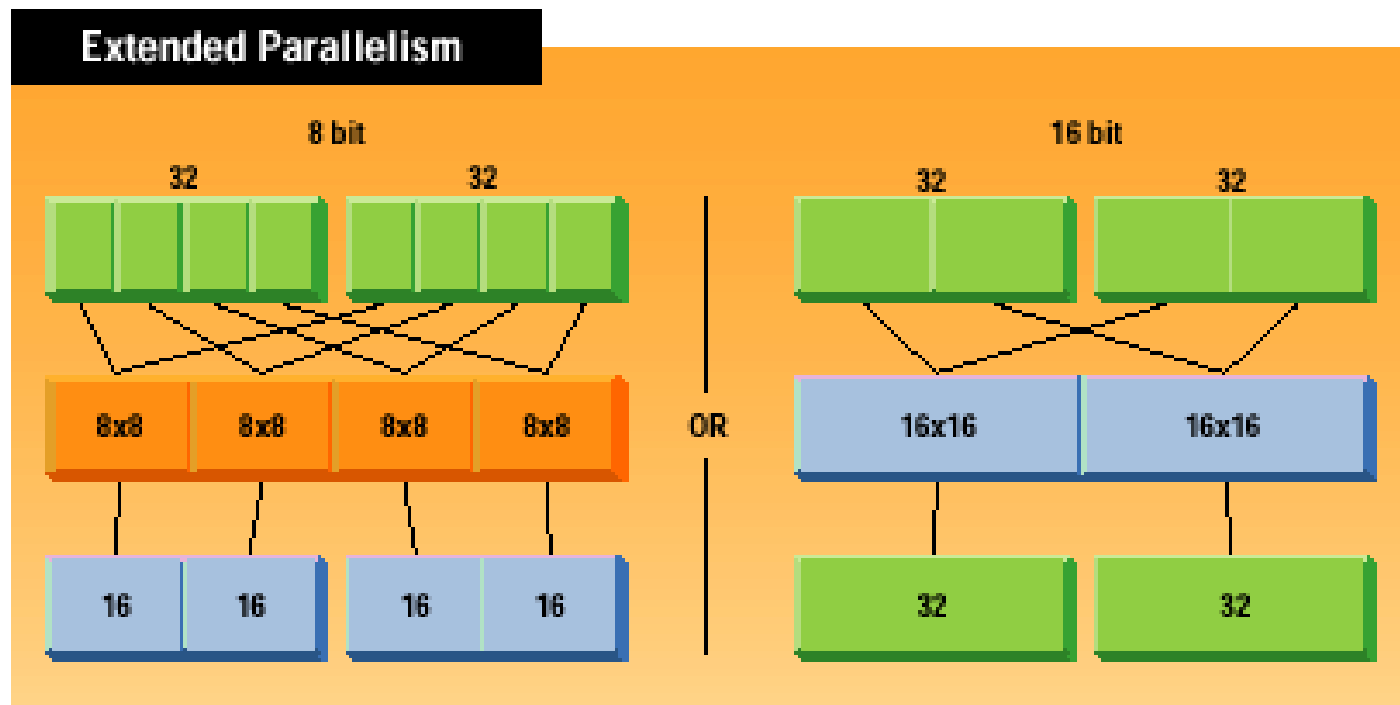
TI TMS320C64x

- VLIW architecture
- Deep pipeline
- 1.1 GHz, 9000 MIPS
- 10X performance of TMS320C62x
- Software compatible with TMS320C6000
- 3G base station
- HDTV



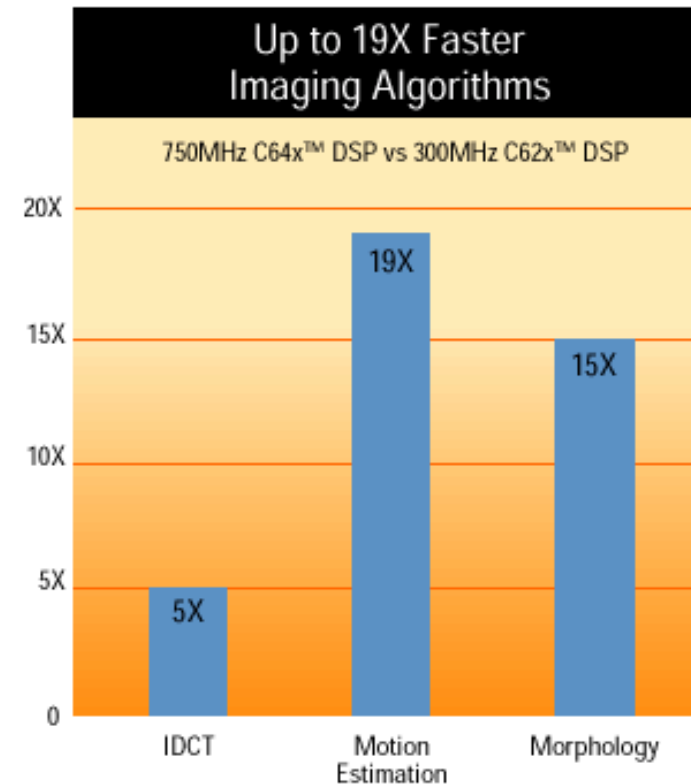
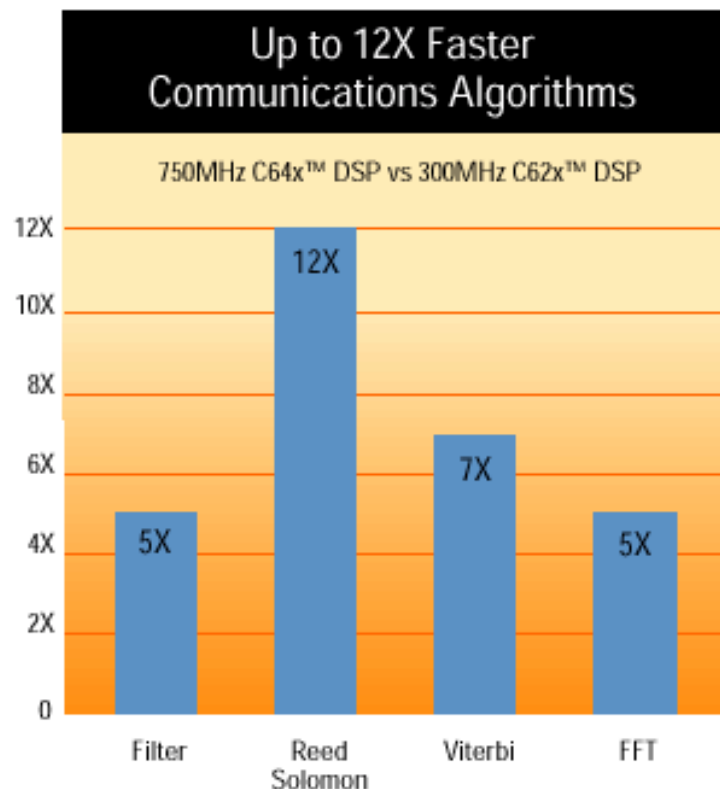
TI TMS320C64x

- Extended Parallelism
 - Four 8x8 multipliers, two 16x16 multipliers, or one 16x32 multiplier



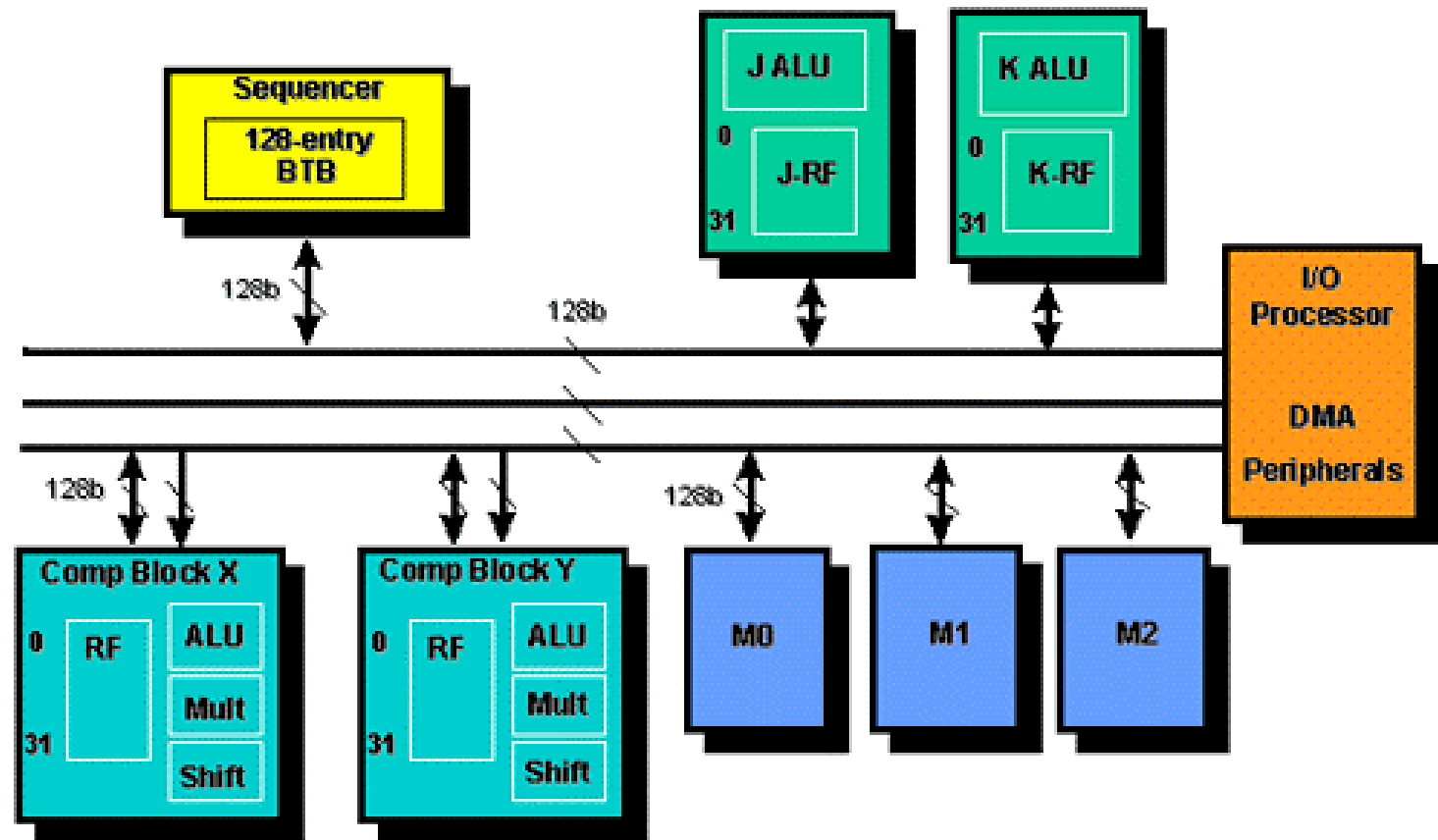
TI TMS320C64x

- New instructions to accelerate digital communication and video applications
 - Error correction code, absolute-difference, ...etc.



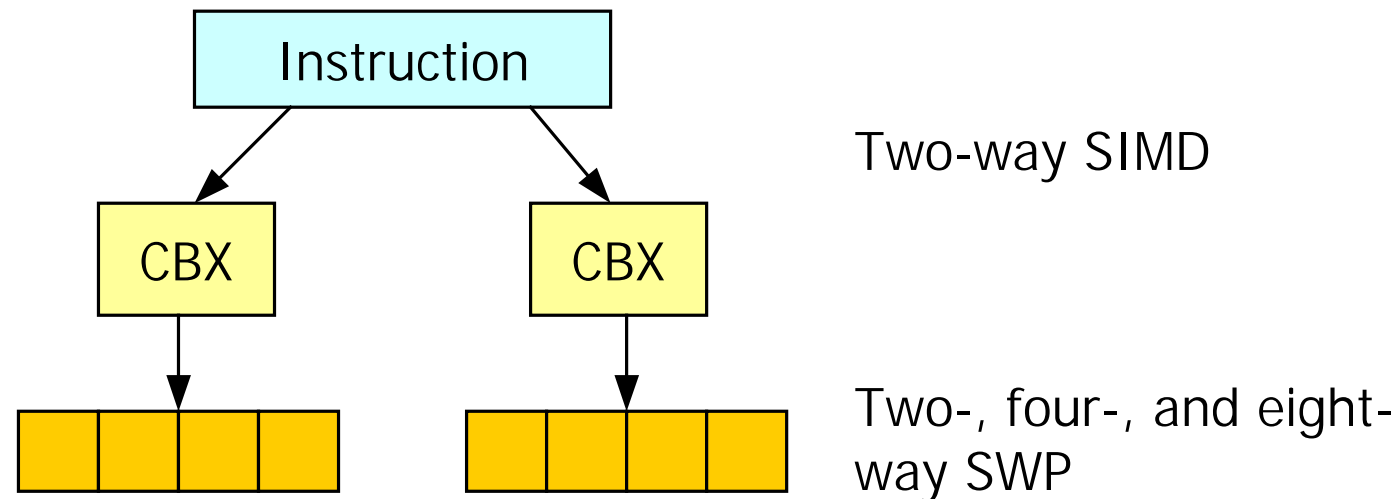
ADI TigerSHARC DSP

- Static super-scalar
- 900 MFLOPS (32-bit floating-point)
- 3.6 GOPS (16-bit fixed-point)



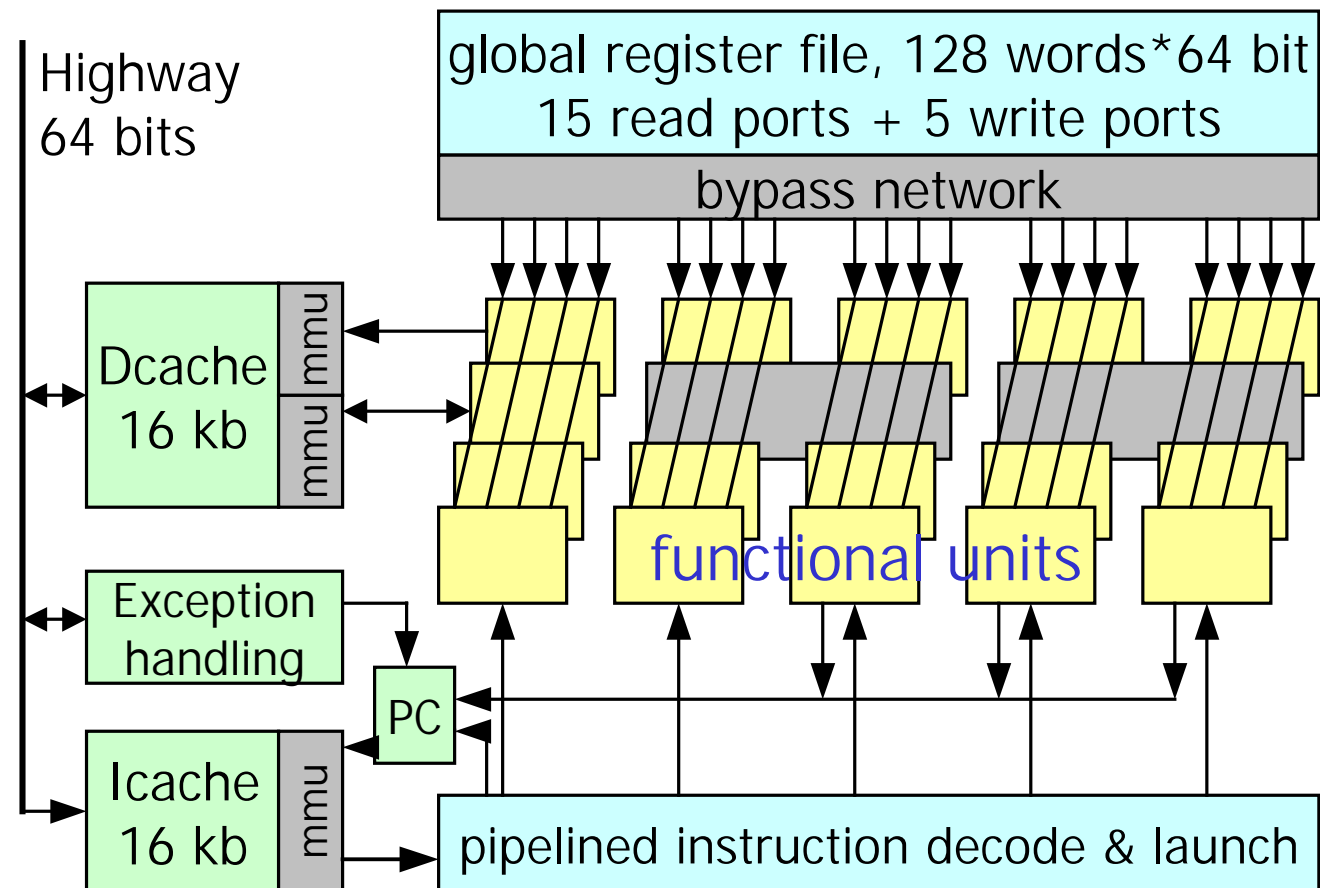
ADI TigerSHARC DSP

- Eight 16-bit MACs, Two 32-bit MACs, or Two 16-bit complex MACs per cycle
- Single cycle Add-Compare-Select (ACS) sequence in the Viterbi algorithm



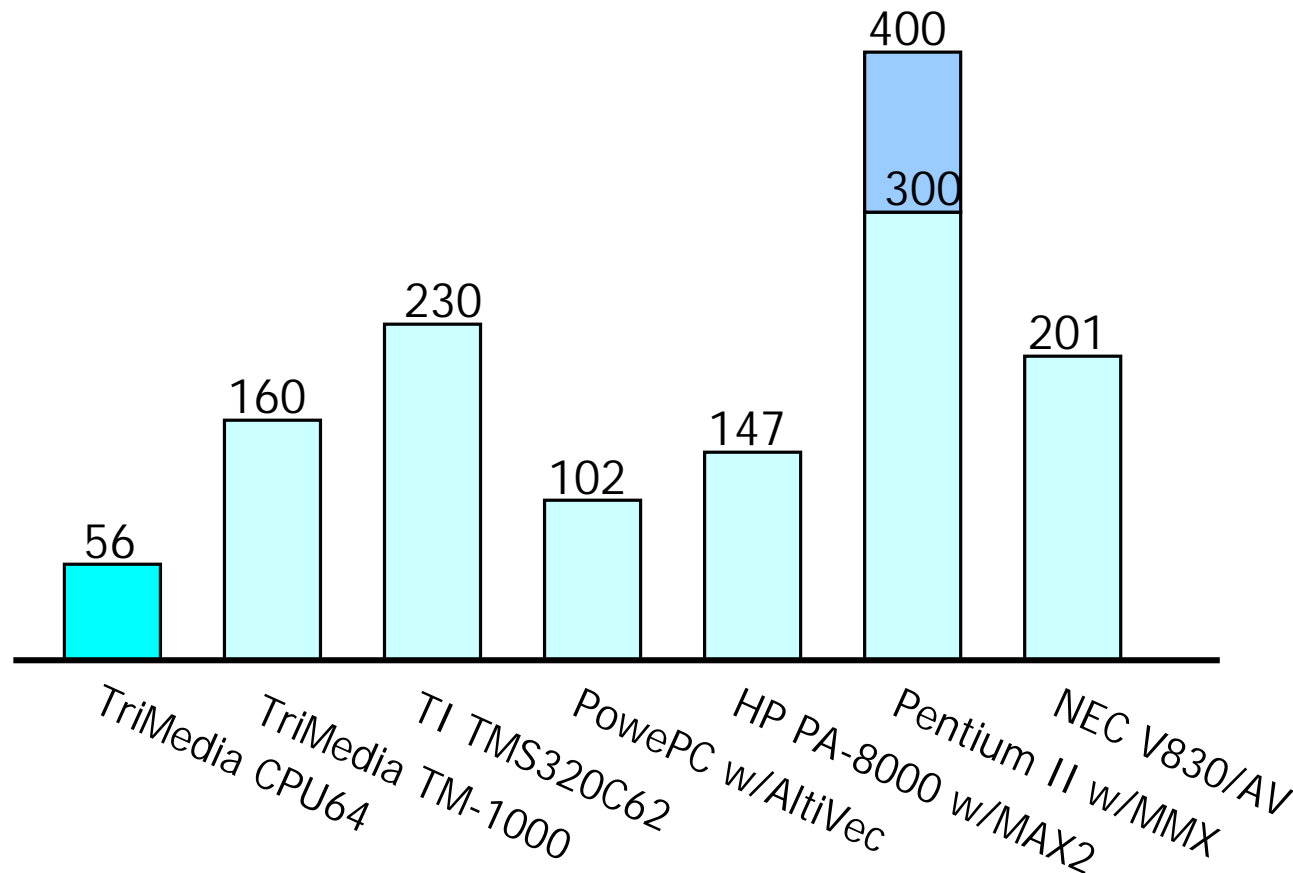
Philips TriMedia CPU64

- Media processor
- 5-issue VLIW with 64-bit word size
- SIMD+SWP
- 27 functional units
- 8-way instruction cache
- 8-way data cache



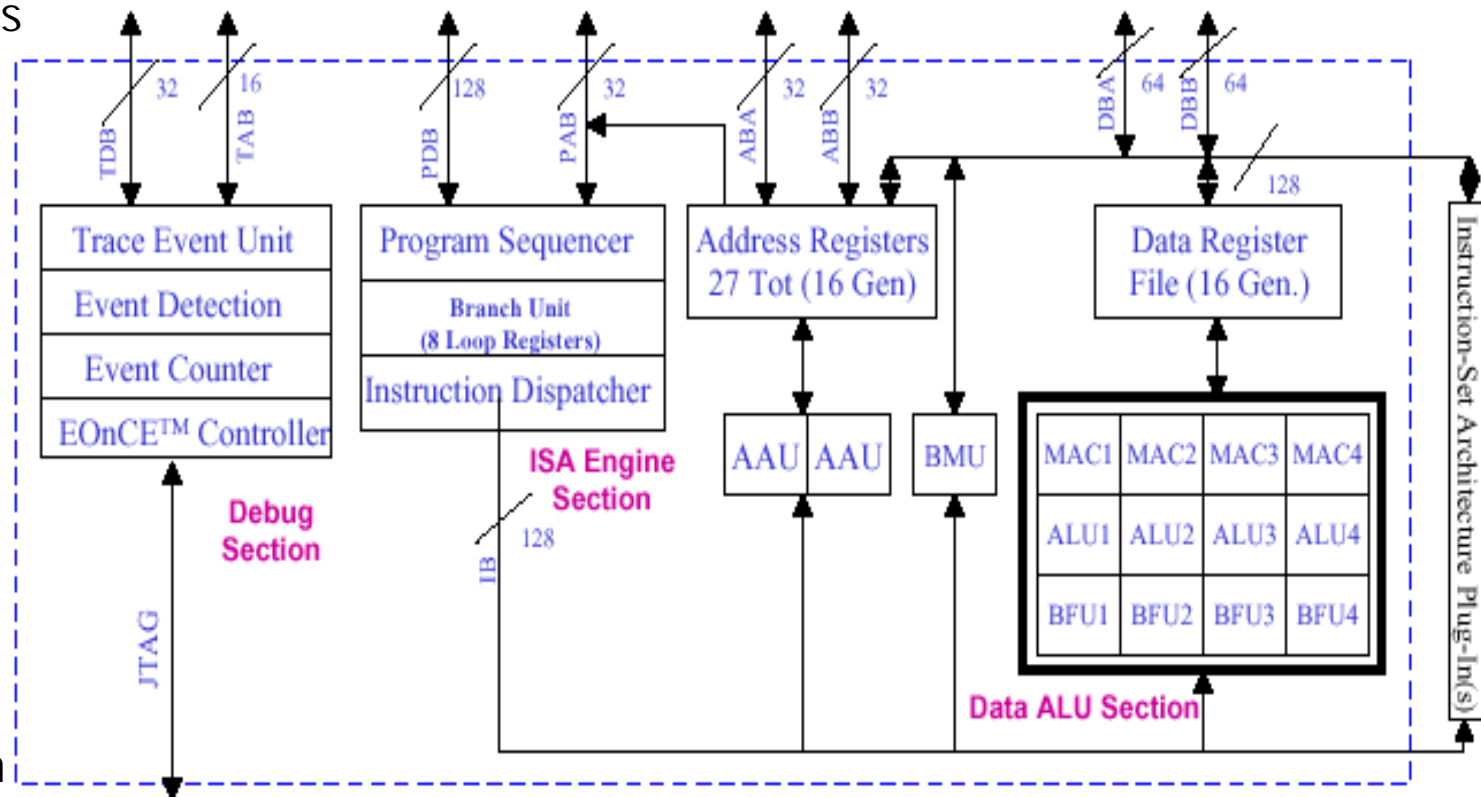
Philips TriMedia CPU64

- VLIW, SIMD, and SWP
 - 8x8 IDCT only needs 56 cycles



Lucent StarCore SC140

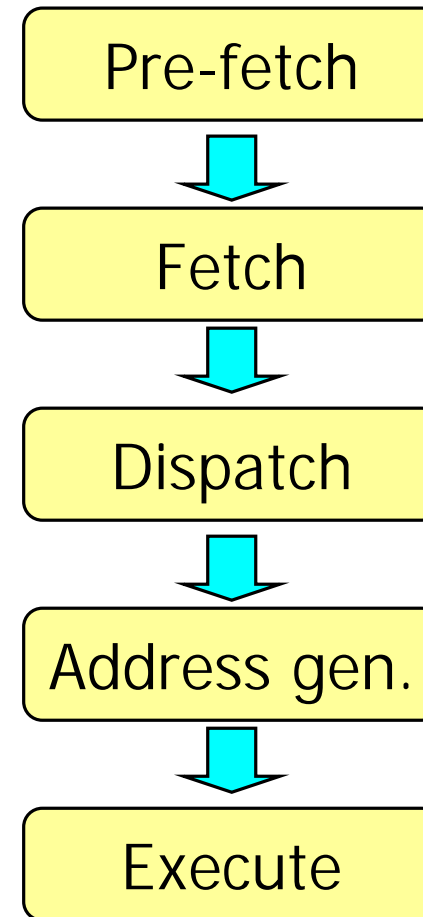
- 1.2 billion MACs
- 3000 RISC MIPS
- Low power, High performance
- 4 ALUs
- Up to 6 instructions per cycle
- Target for 3G wireless communication



Lucent StarCore SC140

■ Pipeline

- Short, Efficient
- No arithmetic interlocks
- Short change of flow
- Simple pipeline hardware
- Every instruction has the same pipeline



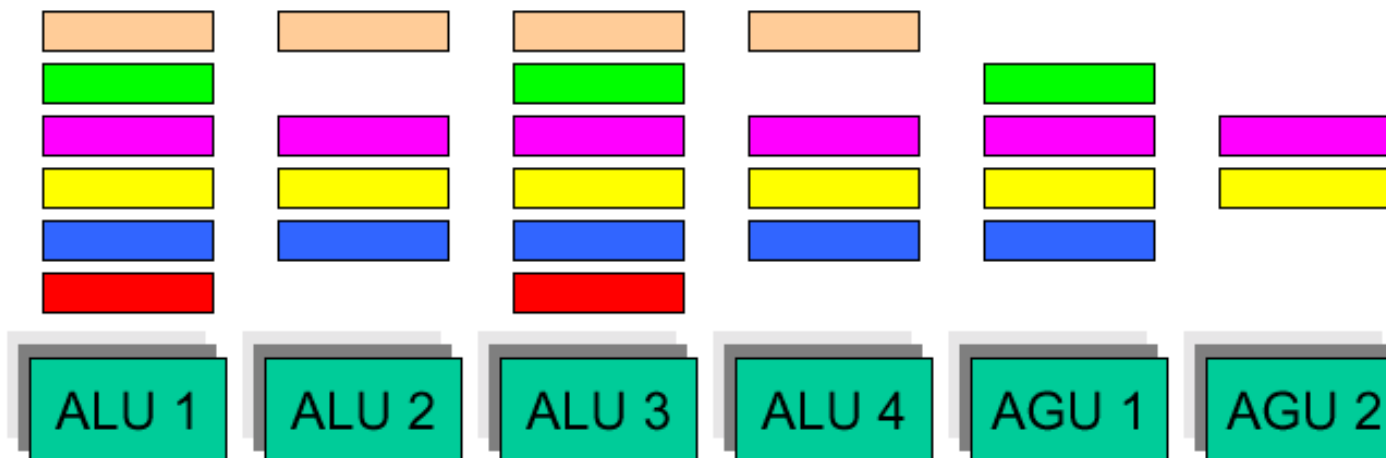
Lucent StarCore SC140

Variable Length Execution Set

- Execution Sets in Fetch Order



- Execution Sets in Dispatch Order

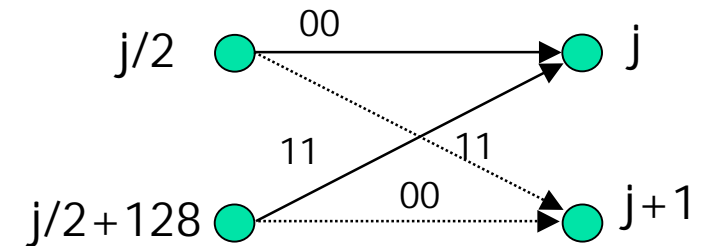


Design Example -- CDSP

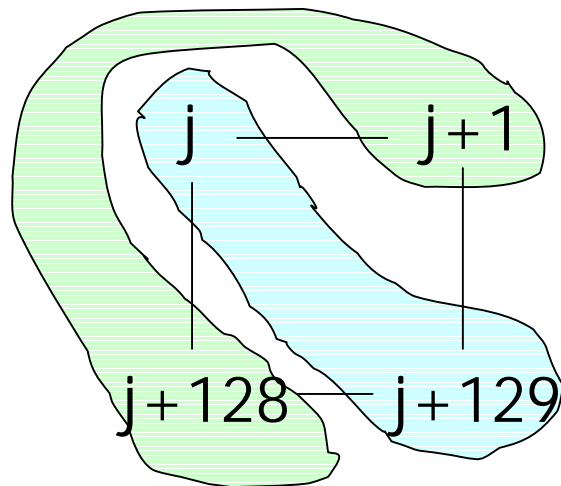
- Domain-specific DSP processor
- Target application domain
 - Third generation wireless communications
 - Wide-band CDMA (WCDMA)
- According to system simulation
 - Special architecture and instruction set
 - SIMD and SWP
 - Memory arrangement consideration

Design Optimization

- ACS Memory Management
 - Use two 1R1W two-port SRAMs



exclusion graph



Metrics

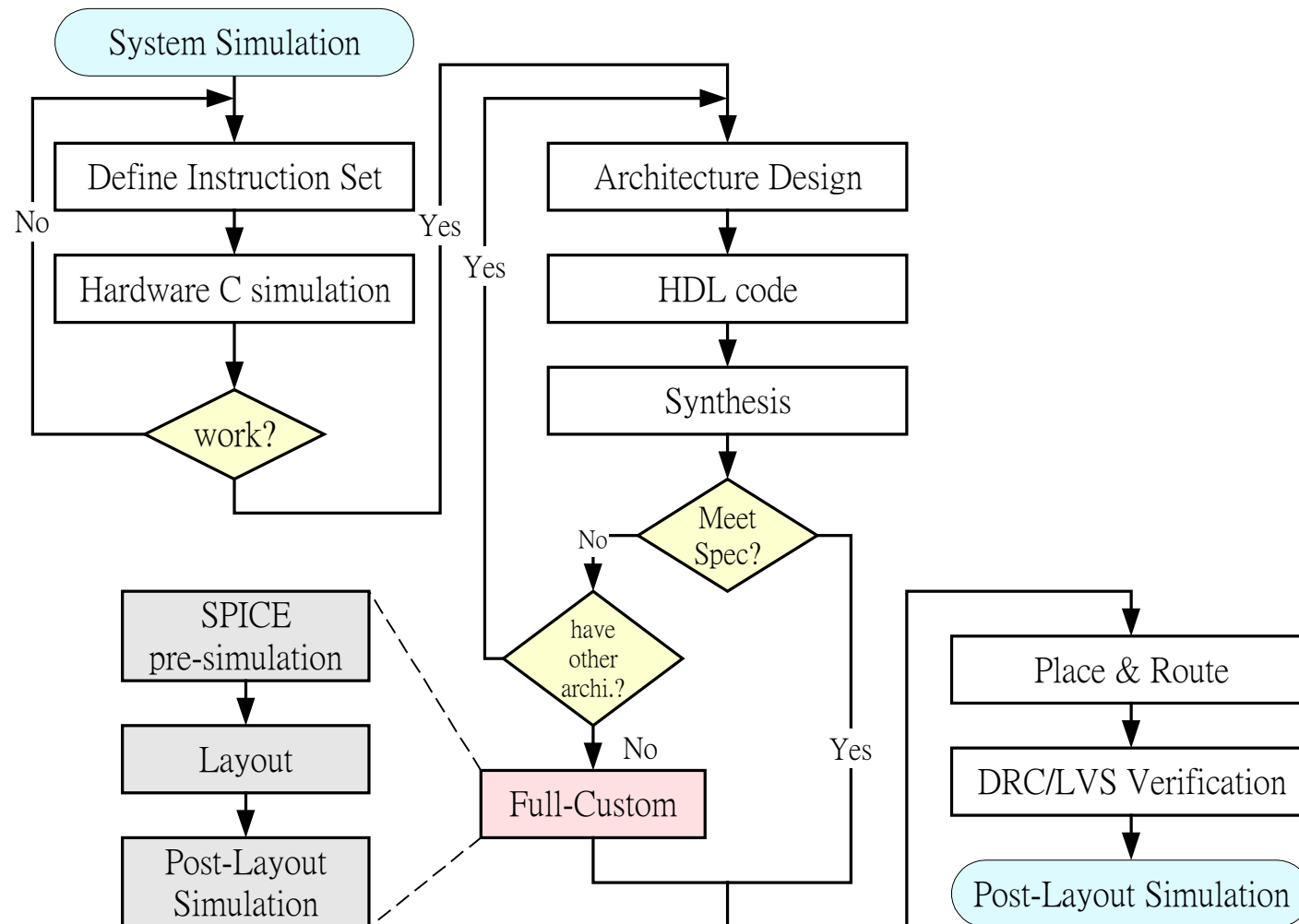
0	1
2	3
.	.
126	127
129	128
131	130
.	.
255	254

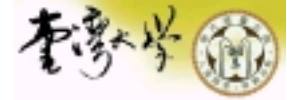
DM0

DM1

j (state number)

Design Flow





Performance Comparison

	TI C54x (1 MAC)	TI C55x (2 MACs)	LODE (2 MACs)	MDSP-II (2 MACs)	CDSP (1 MAC)
GSM Conv. (K=5)	0.58 MIPS	0.276 MIPS	0.44 MIPS	0.8 MIPS	0.093 MIPS
IS-95 Conv. (K=9)	6.57 MIPS	3.13 MIPS	5.2 MIPS	9.01 MIPS	1.38 MIPS
3G Conv. @ 384 kbps	263 MIPS	121 MIPS	208 MIPS	360 MIPS	55 MIPS
FIR (N-tap)	N cycles	N/2 cycles	N/2 cycles	N/2 cycles	N/2 cycles
Complex MUL/MAC	4 cycles	2 cycles	2 cycles	2 cycles	1 cycle

Future Trends

- New architecture
 - Hardware accelerator plug-in
 - More parallelism & special purpose
- Configurable-Length-Instruction-Word
 - Customized instruction set DSP processors
- On-chip programmable logic
 - Re-Configurable computing system
- Embedded system software