

The Technology Trend of Embedded Processor

A decorative graphic on the left side of the slide, consisting of overlapping blue, red, and yellow squares with a black crosshair.

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Outline

- Introduction
- Applications and Market Requirements
- Domain Specific Processing
- Current Embedded Processors
- DSP Processor Fundamentals
- DSP/MCU/MPU Issues

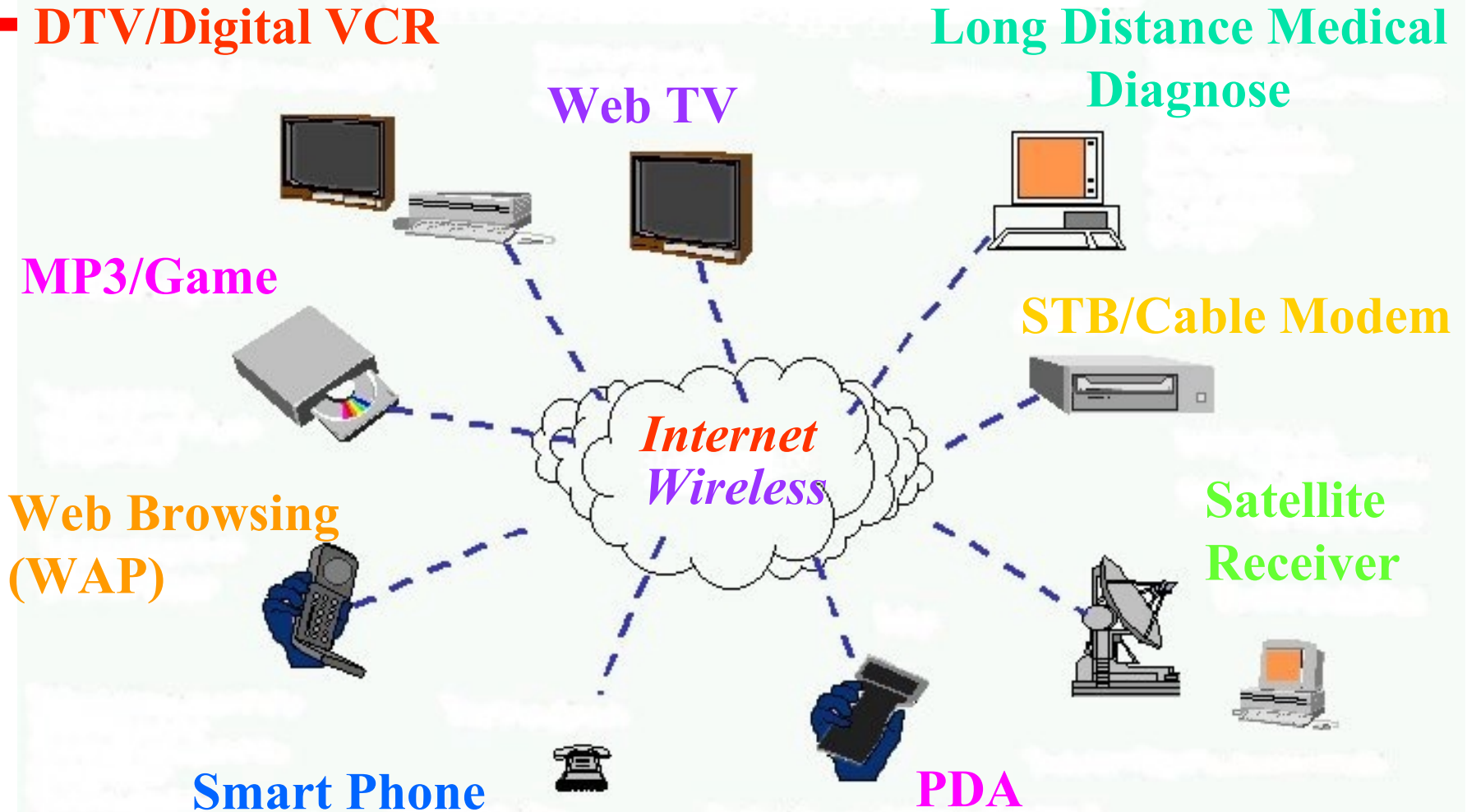
Introduction

- What is Embedded System?
 - W. Wolf : “Any sort of device which includes a programmable computer but itself is not intended to be a general-purpose computer.”

Applications and Market Requirements

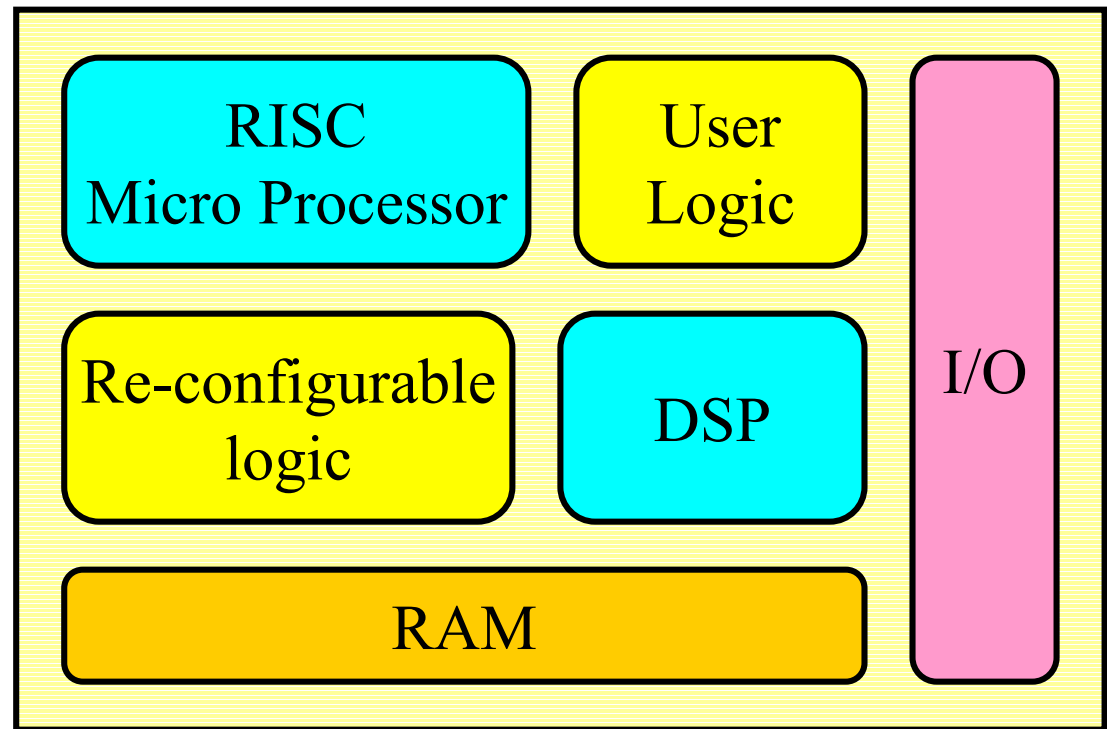
- Video game consoles
- Handheld, palmtop, automobile, and network PCs
- Cellular phones
- Video phones
- Modems, fax machines
- Set-Top boxes and DVD
- Digital cameras
- MP3 players
- ADSL/HDSL
- Radio decoders
- Answer machines
- Cable modem
- Digital hearing aids
- Cordless phones
- Voice over IP

Information Appliance

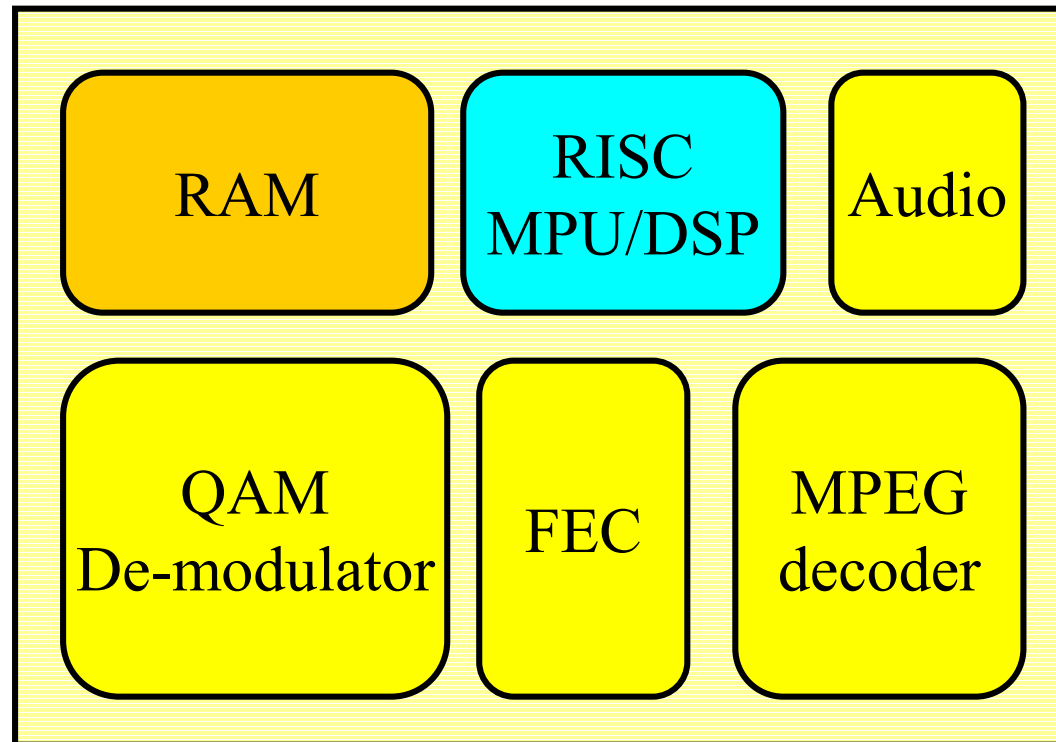


Integration will be the perfect solution

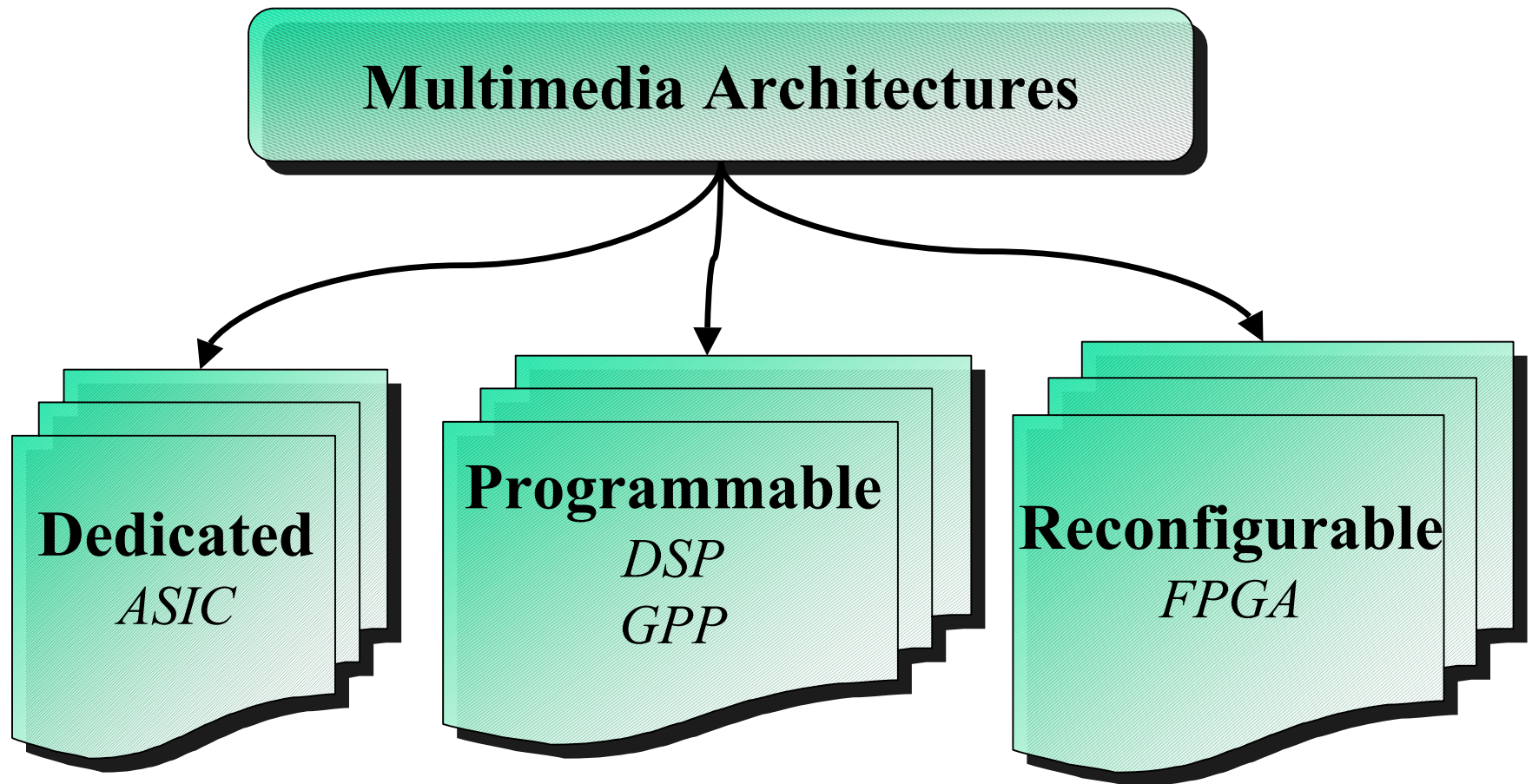
- Time to market
- High volume
- System – On – Chip



Example: STB chip



Multimedia Architectures



Today's DSP Landscape

- **Low-cost workhorses: 20-50 MIPS**
 - ADSP-21xx, TMS320C2xx, Motorola's DSP560xx families
- **Low-power midrange: 100-120 MIPS**
 - Lucent's DSP 16xx, TMS320C54x
 - increased clock, deeper pipelines
- **Diversified high-end: ~1000 MIPS**
 - Enhanced conventional DSP processors: more parallel units
 - Multiple instruction issue: mostly VLIW

Programmable

**Enhanced
Conventional
DSP**

Lucent DSP16xxx

Superscalar

NEC V830R/AV

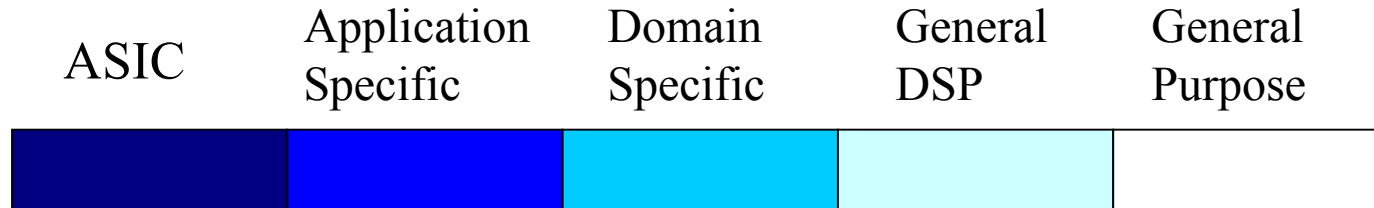
**VLIW-
based**

*TI TMS320C6xxx
Philips TriMedia
Sun MAJC*

GPP

*Intel MMX
AMD 3D Now!*

Domain Specific Processors



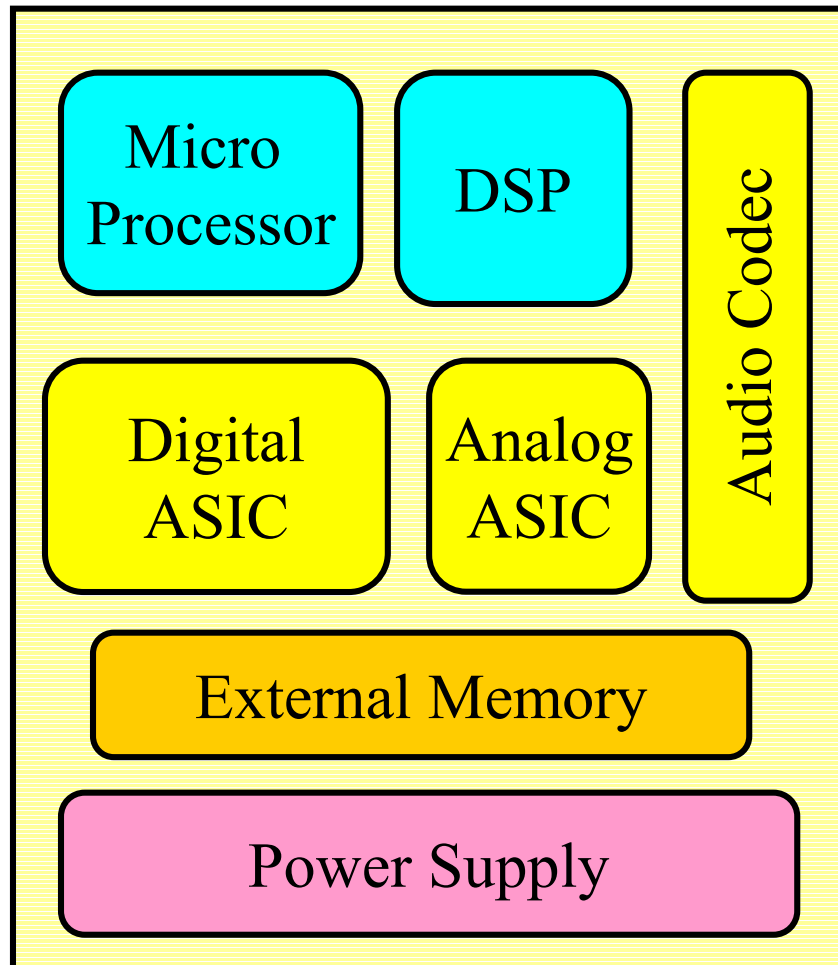
Performance / Power :



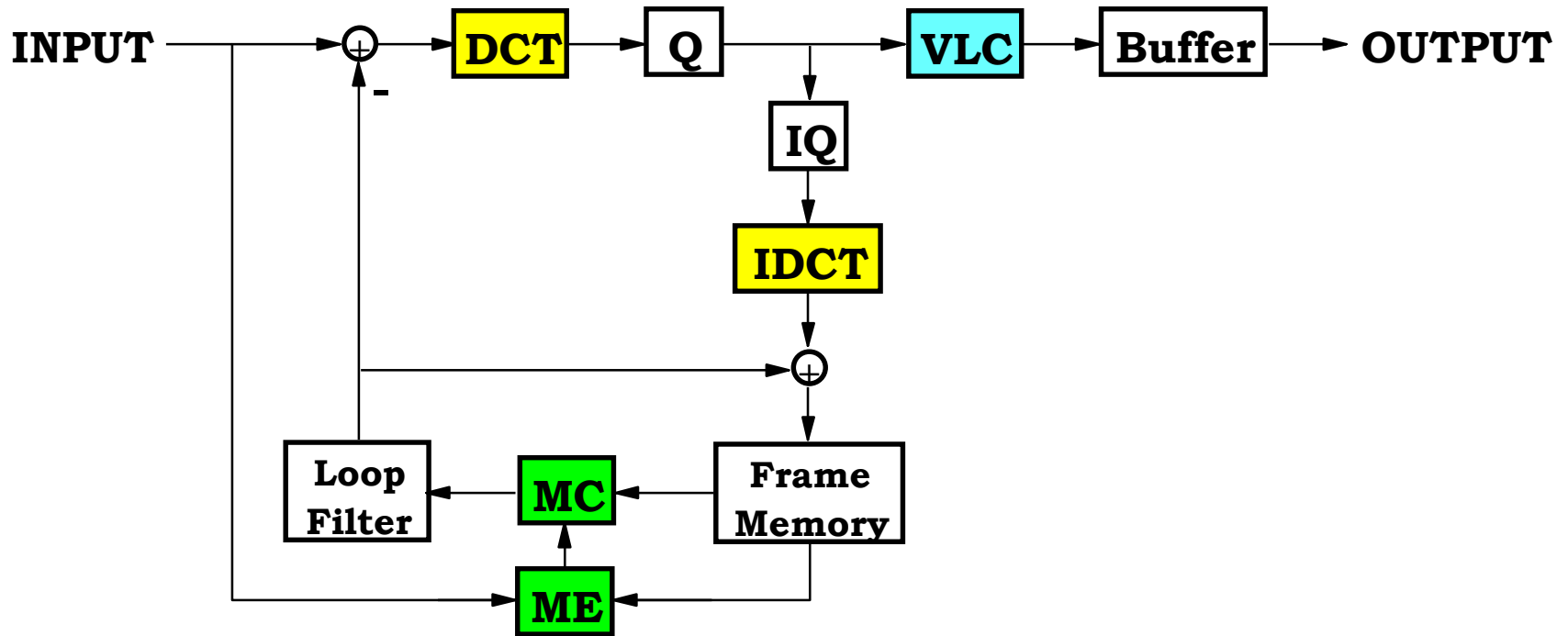
Programmability:



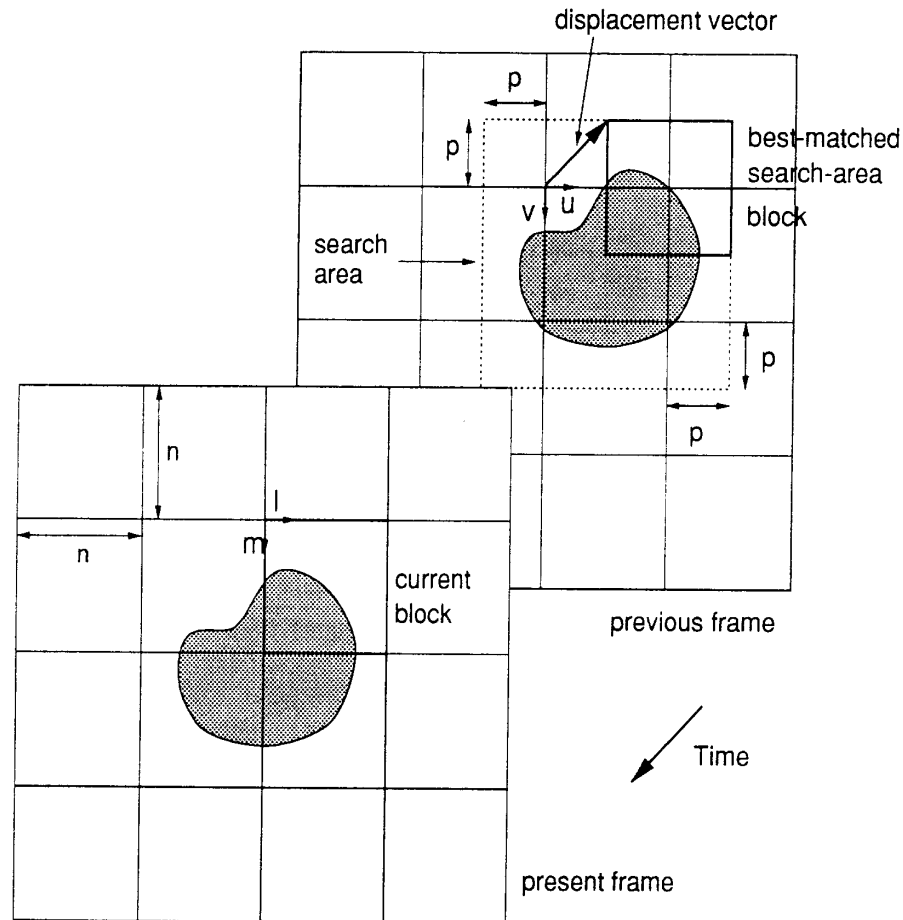
Application domain: video phone



A Typical Video Compression System



Motion Compensation/Estimation



Discrete Cosine Transform

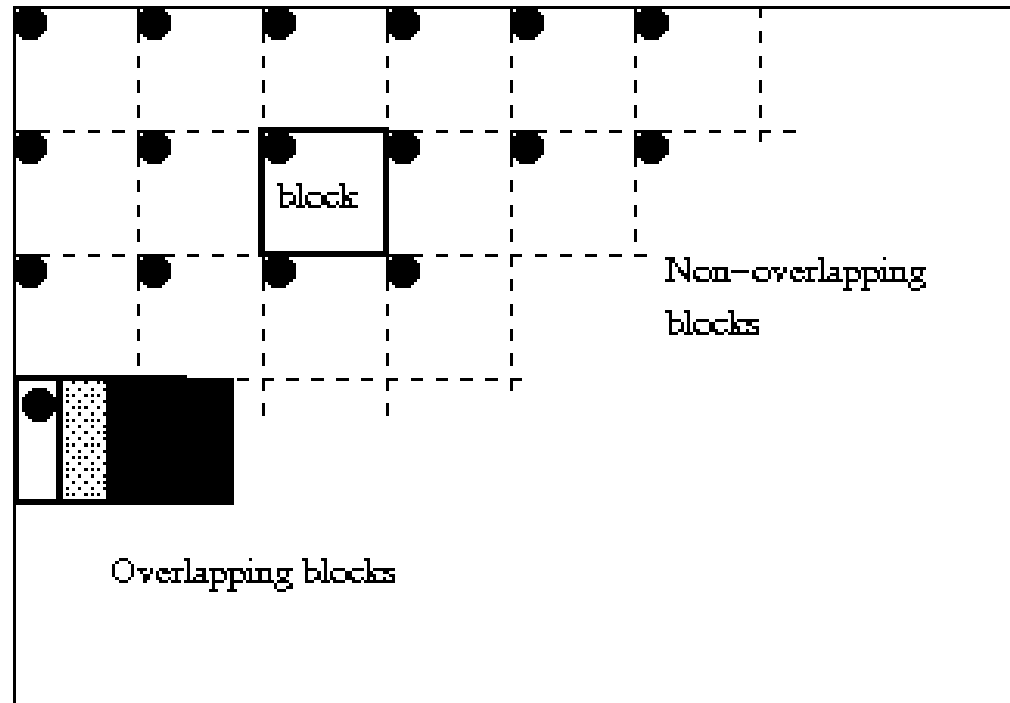
- Block size: 8 x 8
- Two-dimensional DCT:

$$F(u, v) = \frac{2}{N} C(u) C(v) \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} f(x, y) \cos \frac{2\pi(2x+1)u}{4N} \cos \frac{2\pi(2y+1)v}{4N}$$

$$C(u), C(v) = \begin{cases} 1/\sqrt{2}, & u, v = 0 \\ 1, & \text{otherwise} \end{cases}$$

- Separable -- row-column method
- Most large coefficients concentrate on the upper-left corner
- Quantization and zig-zag scan

Block-Oriented Data Access



frame

● : Pixel

Typical Video Signal Processing

TYPICAL VIDEO SIGNAL PROCESSING

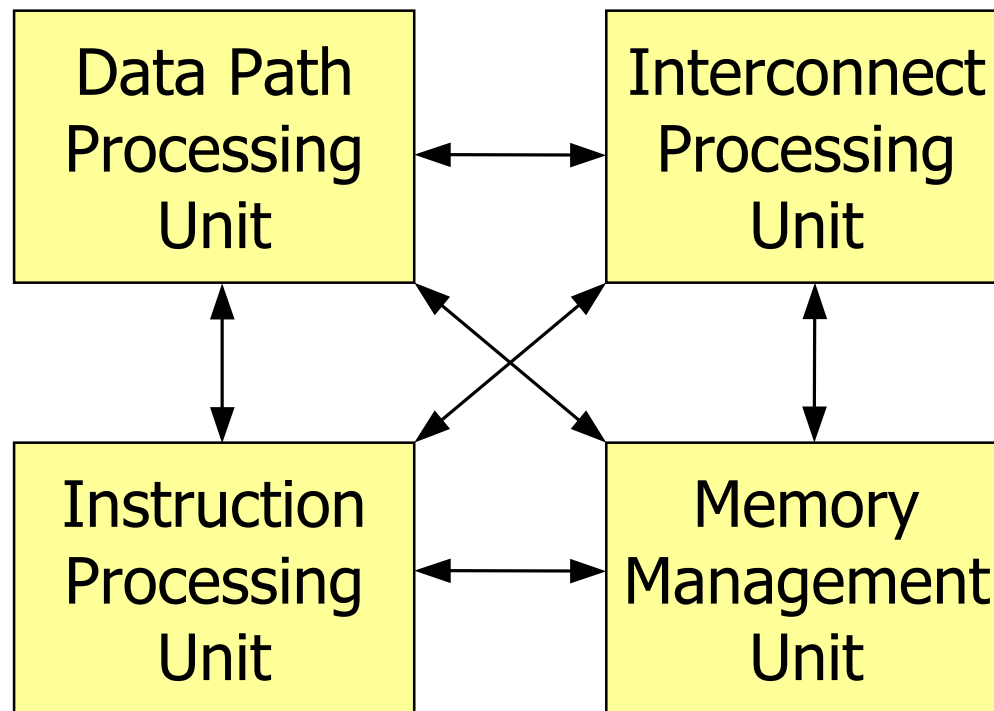
Processing	Operation	Addressing
Motion Estimation	$\Sigma x - y $ or $\Sigma(x - y)^2$	2-D block (Sliding)
Transform Coding	$\Sigma a \times x$	2-D block
Vector Quantization	$\Sigma a \times x$ or $\Sigma(x - y)^2$	2-D block
Convolution	$\Sigma x \times y$	2-D block (Sliding)
Filtering	$a \times x + b$	2-D block
FFT	$a \times x + b$	Bit Reverse

Application Domain: evolution of Processors

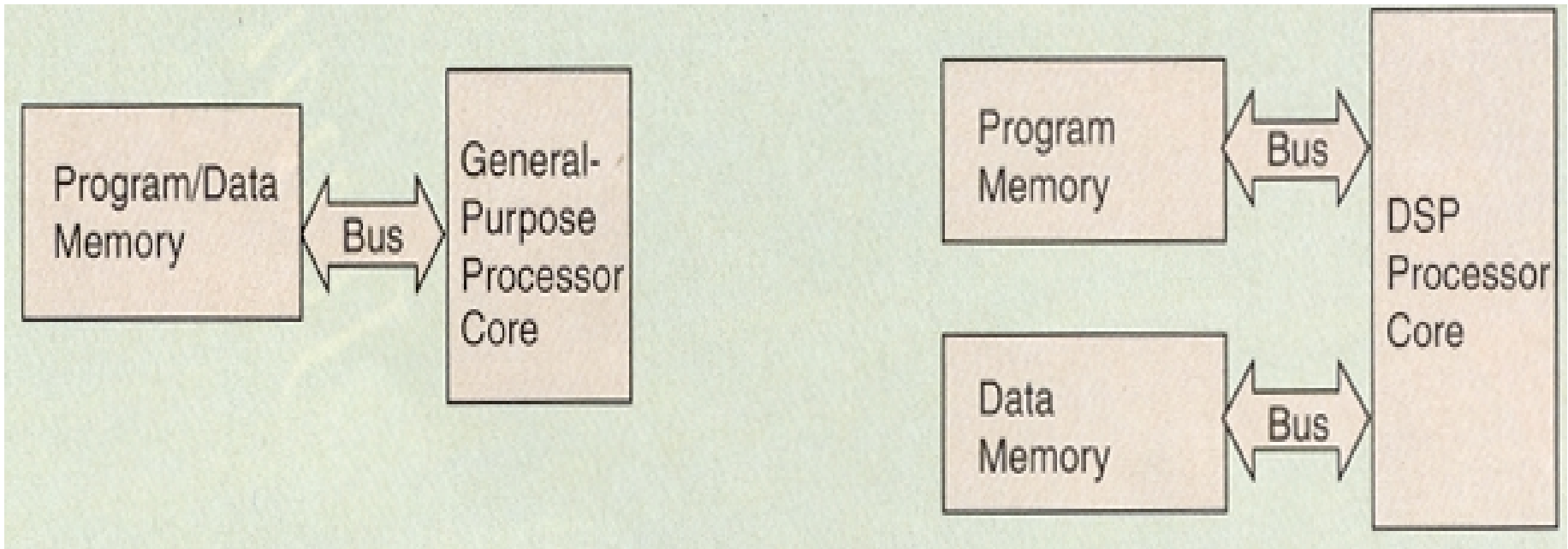
- Low power designs
- Speed-up of FIR
- Viterbi acceleration
- Square distance
- Video Processing

DSP Processor Fundamentals

- Processor Components

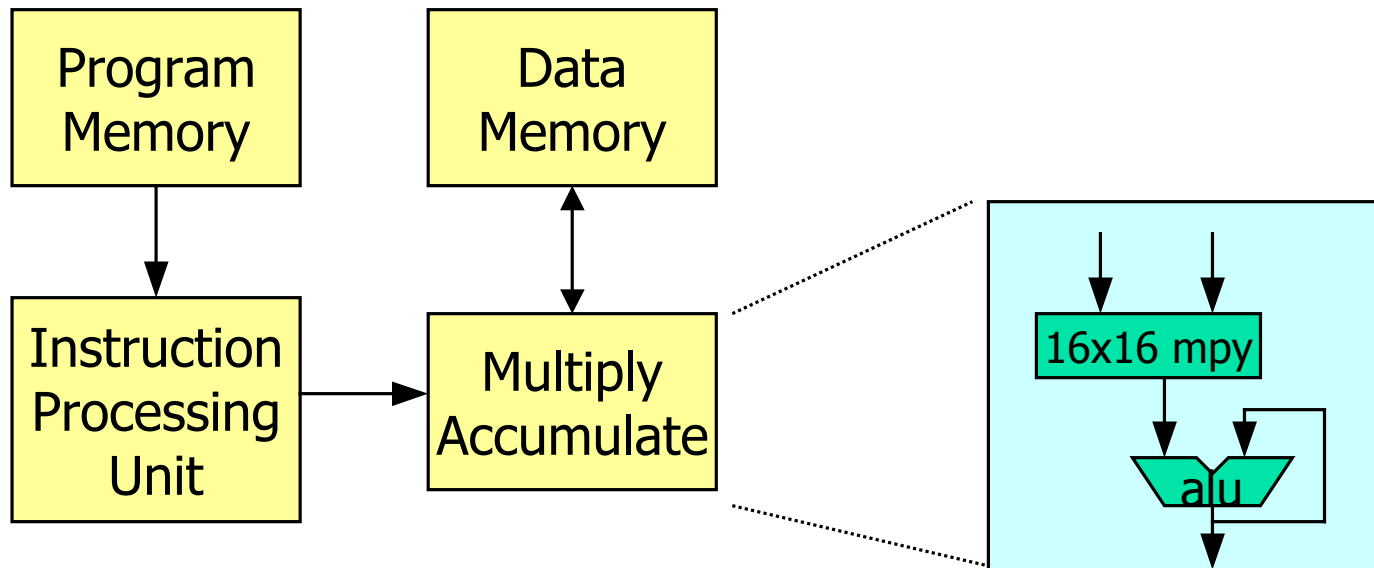


Differences in Memory Architectures for DSP and MPU



Basic Harvard Architecture

- Separate data memory from program memory



- Different from Von Neumann machine:
 - One address bus – one data bus – one memory space

DSP Architectures Specialty

- Fast Multipliers
- Multiple Execution Units
- Efficient Memory Accesses
- Data Format
- Zero-Overhead Looping
- Streamed I/O
- Specialized Instruction Sets

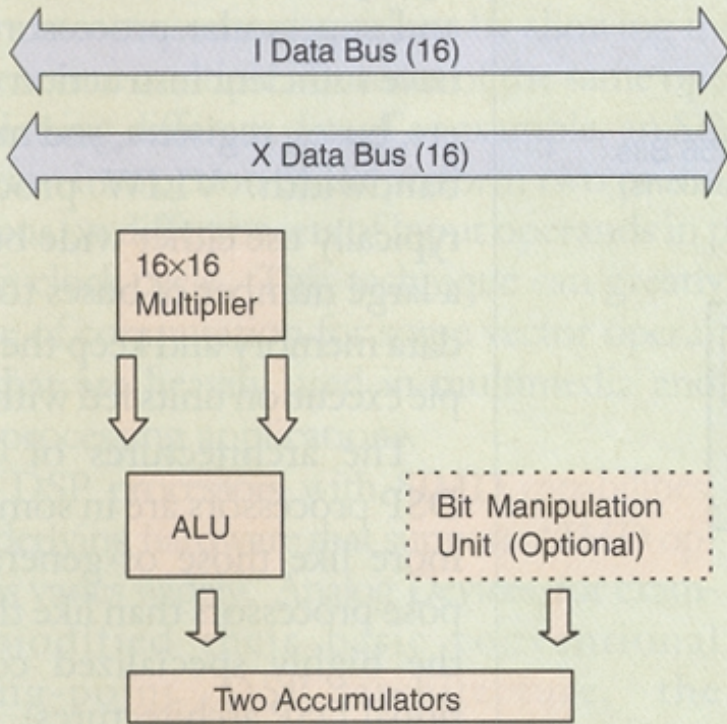
Evolution of DSP Processors

Generation	Features	Examples
0 (1980)	Von Neumann architecture	DSP-1 (AT&T)
1 (1982)	Basic Harvard architecture	TMS320C10 (TI) NEC7720
2 (1986)	1 data/program bus, 1 data bus	TMS320C25 (TI) DSP16A (AT&T)
3 (1990)	Extra Addressing modes, extra functions	TMS320C5X (TI) DSP16xx (AT&T)
4 (1994)	2 data busses, 1 program bus	TMS320C54X (TI)
5 (1996-now)	2 data busses, 1 program bus, multiple units	Lucent 16xxx Atmel Lode Siemens Carmel

Embedded Processors Examples

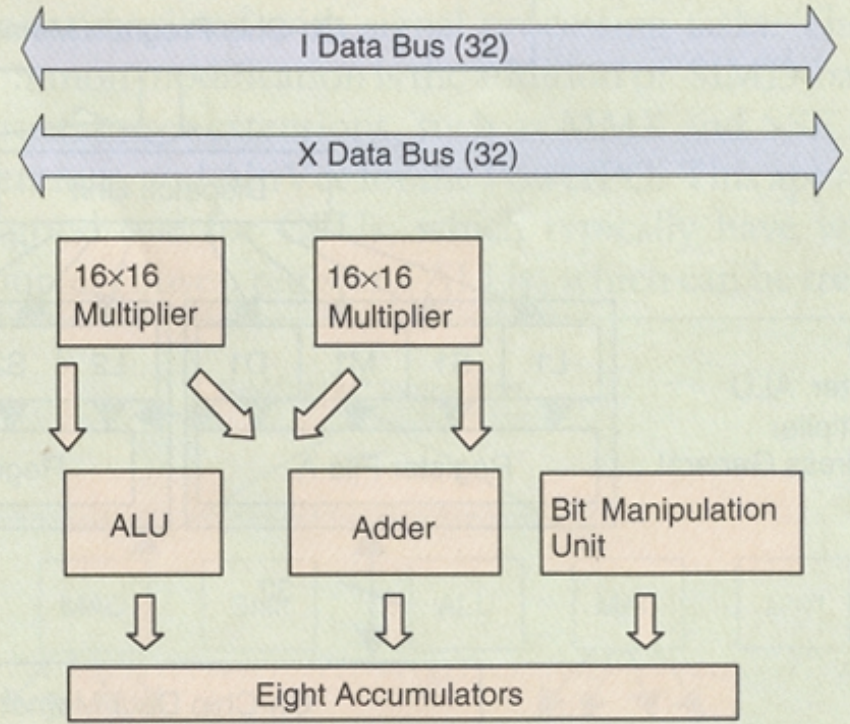
- Intel 8051
- Intel x86, i960
- Intel StrongARM
- ARM, Thumb
- TI C54,C55,C64
- Motorola M*CORE
- Motorola Coldfire
- Motorola 68HC11
- IBM Power PC
- Lucent StarCore SC140
- Transmeta Crusoe
- Hitachi SH2, SH3
- SHARC DSP
- Fujitsu FR-V
- Sun Ultra-Sparc
- National Geode SC1400
- DSP Group Teak, Oak
- SandCraft SR1-GX
- MIPS

DSP Landscapes



(a)

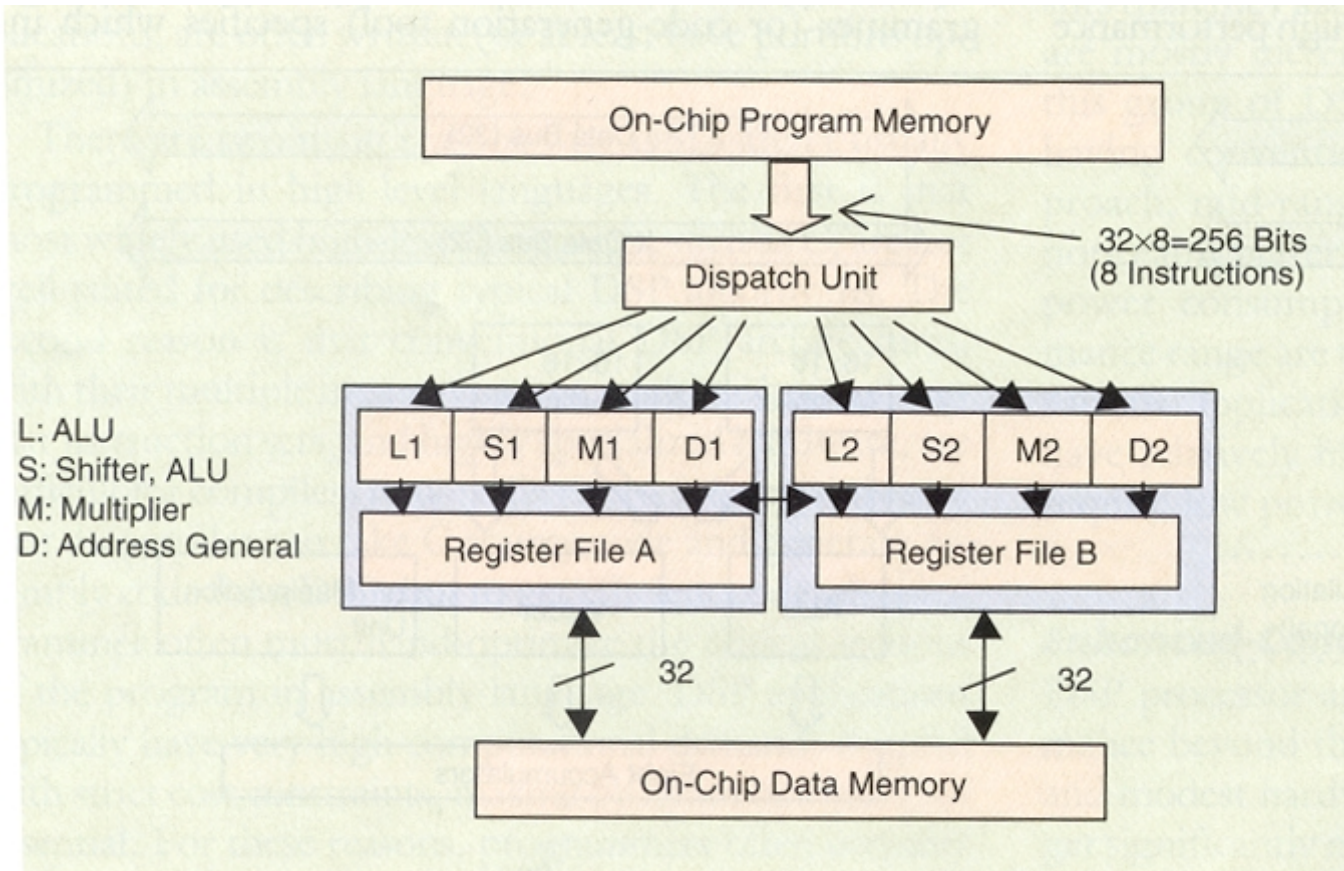
Conventional DSP Processors



(b)

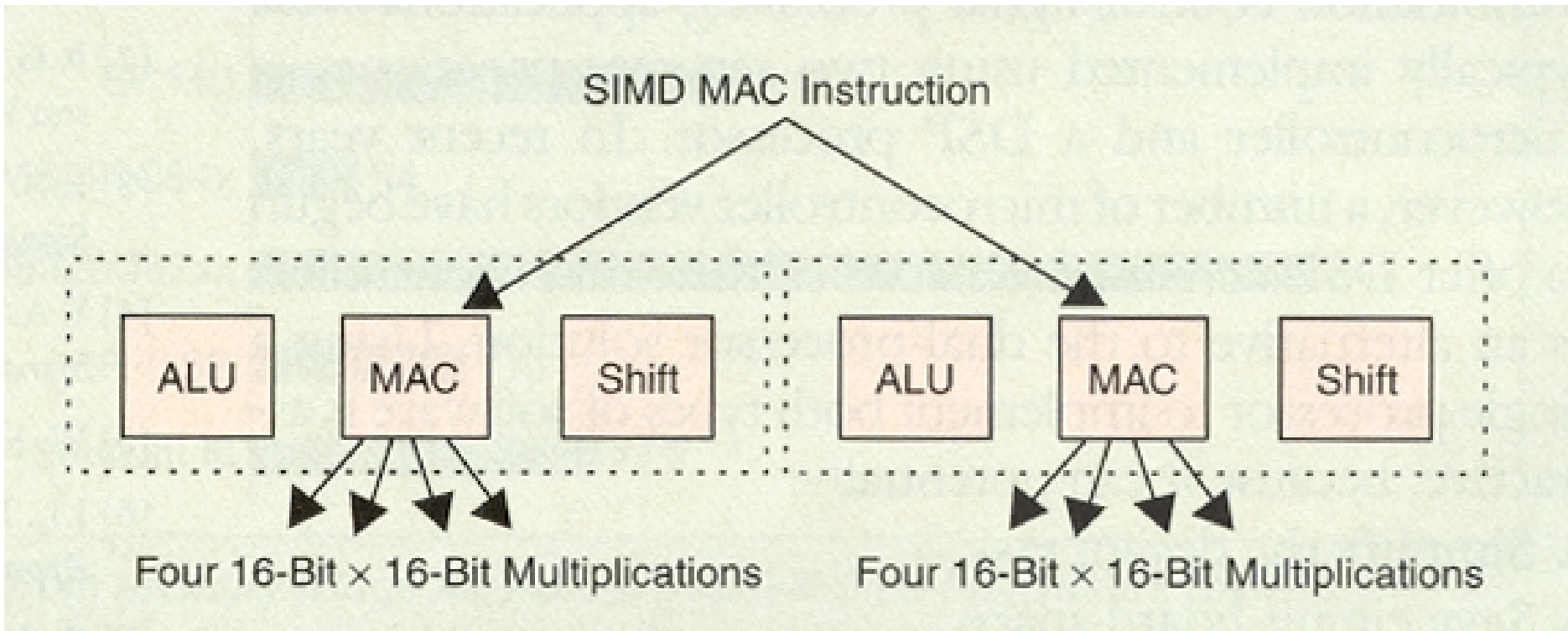
Enhanced-conventional DSP Processors

DSP Landscapes



TMS320C62xx execution units and memory architecture

DSP Landscapes



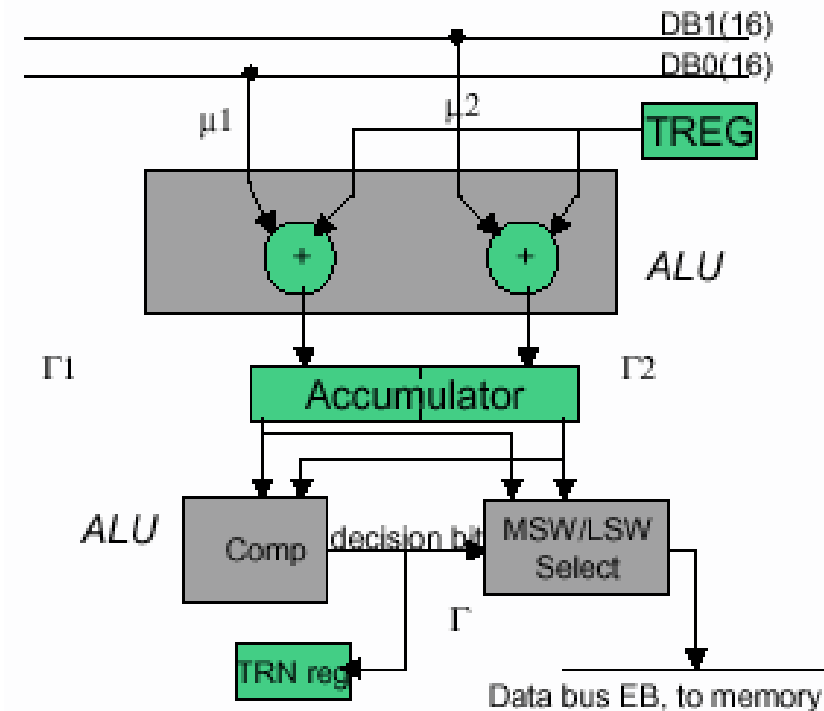
TigerSHARC's SIMD features

TI C54

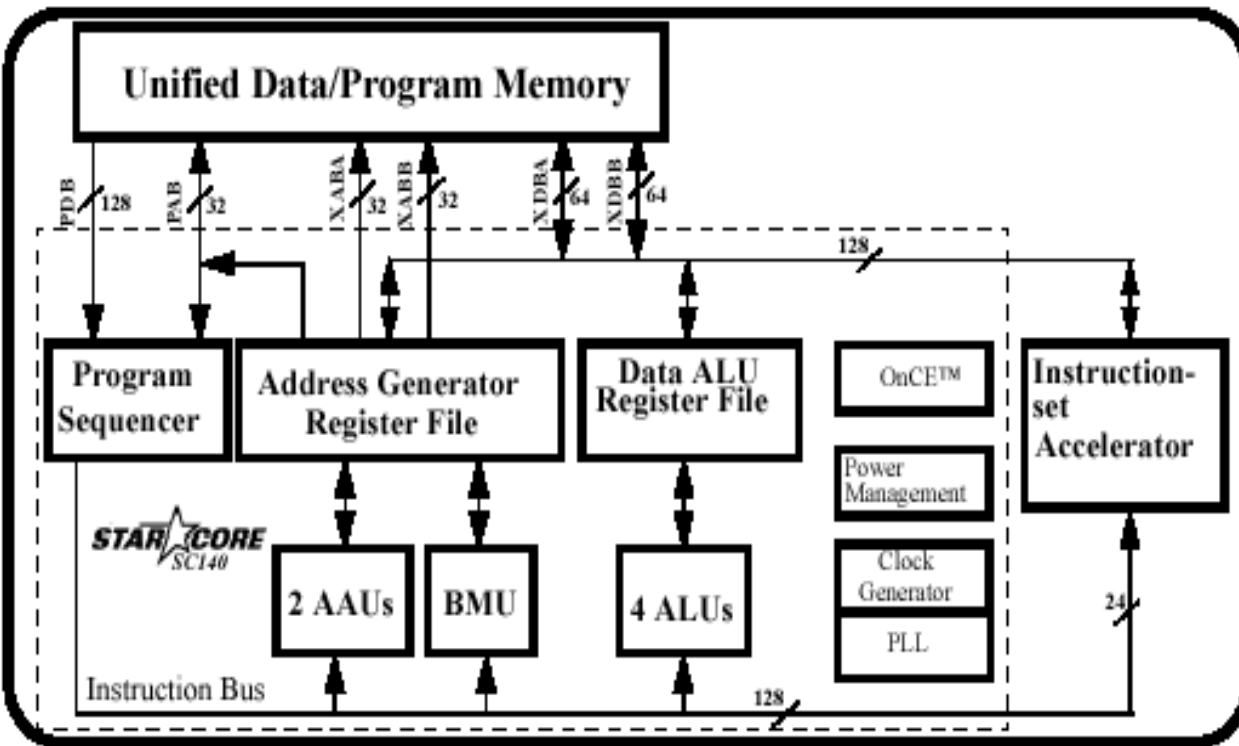
■ Viterbi Accelerate – ALU and CSSU: ACS

$$\Gamma = \min [(\Gamma_1 + \mu_1), (\Gamma_2 + \mu_2)]$$

- ALU splits in 16 bit halves
- ACC splits in half
- Shortest distance saved
- CSSU compares halves
- Path indicator saved
- 4 cycles/butterfly



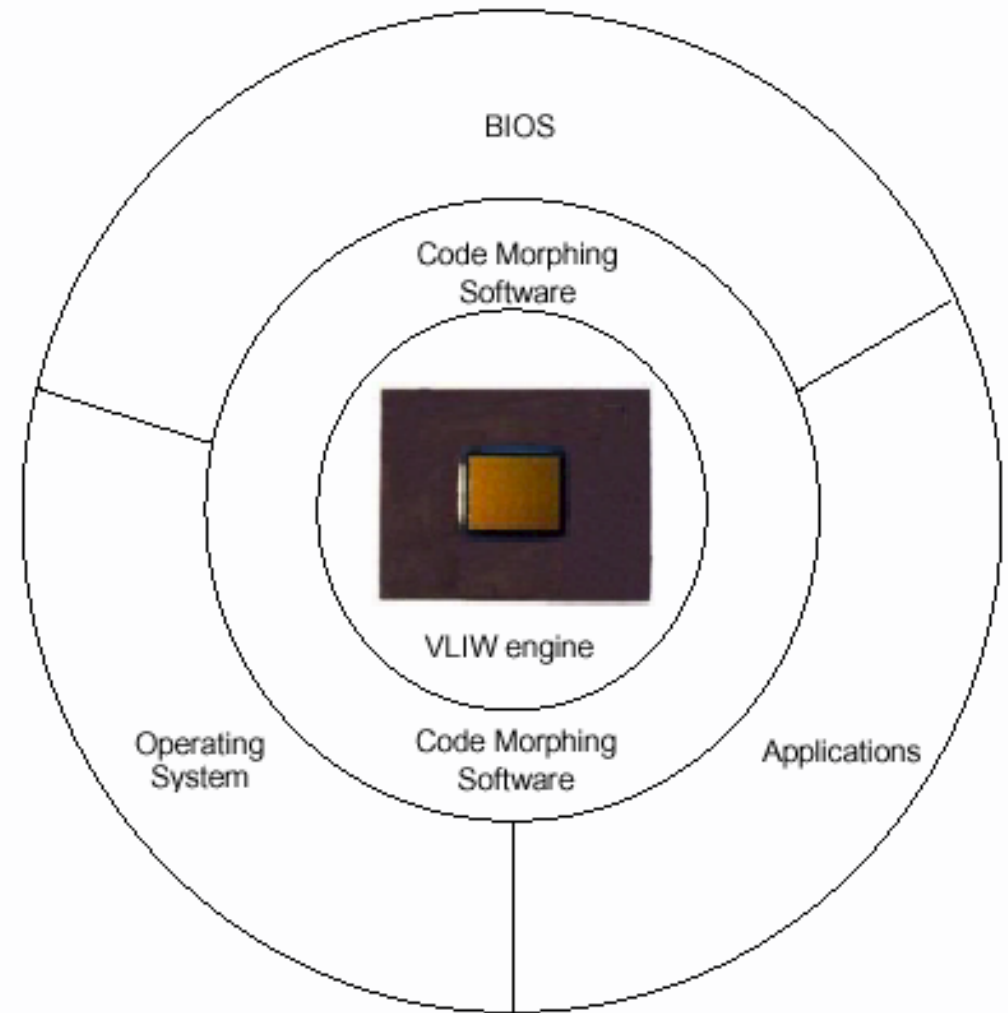
Lucent StarCore SC140



- Variable length instruction set
- 1.2 billion MAC/s
- 3000 RISC MIPS
- Execute 6 instructions per cycle
- Low power, static CMOS design

Transmeta Crusoe

- X86-compatible
- For mobile app.
- Software-based
- VLIW core
- Low-power



Low Power DSPs

■ StarCore SC140

- 0.06mW/MIPS at 0.9V
- 1200M MACs/3000 RISC MIPS at 300MHz (198mW total) at 1.5V
- Variable instruction length

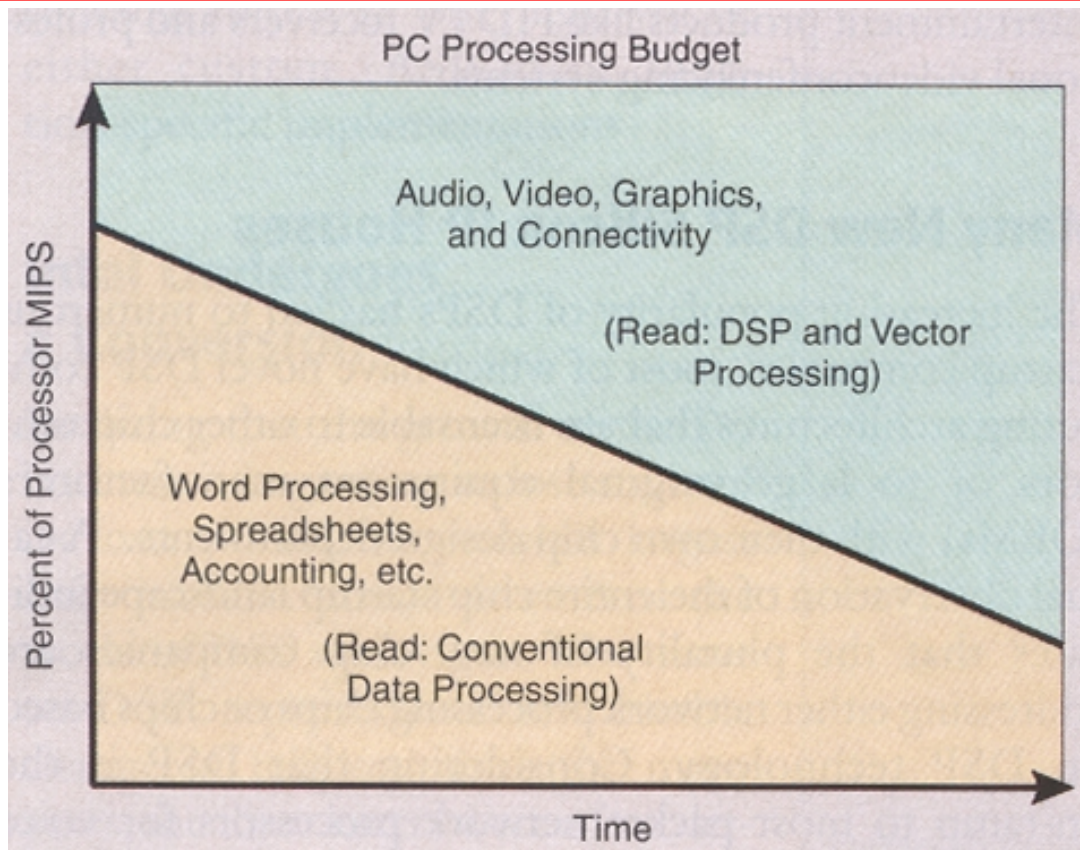
■ TI C55x

- 0.05mW/MIPS at 0.9V
- 800M MACS at 400Mhz (64mW total at 1.5V)
- Variable instruction length

High performance DSPs

- TriMedia CPU64
 - 64bits, 5-issue VLIW architecture
 - 27 function units
 - 32 kB, 8-way instruction cache
 - Variable length instruction set
- TI C64
 - 8 function units
 - 64 bits data path
 - Two level cache
 - 1.1GHz, 8800MIPS
- StarCore SC140
 - 12000 MIPS
 - Variable length instruction set
 - 4 ALUs

DSP/MCU/MPU Issues



Application is driving processors to handle increasing audio, video, and graphics capability for the internet connectivity.

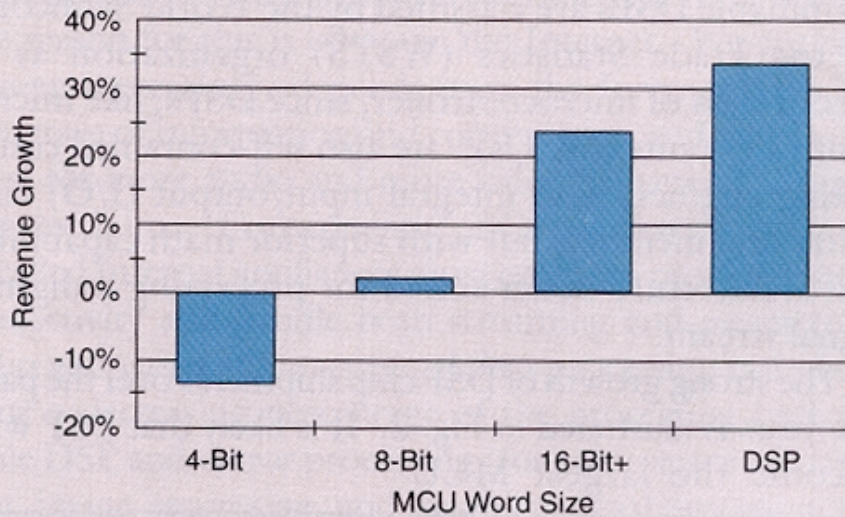
DSP Additions to Traditional MPUs

Table 1. DSP Additions to Traditional MPUs.

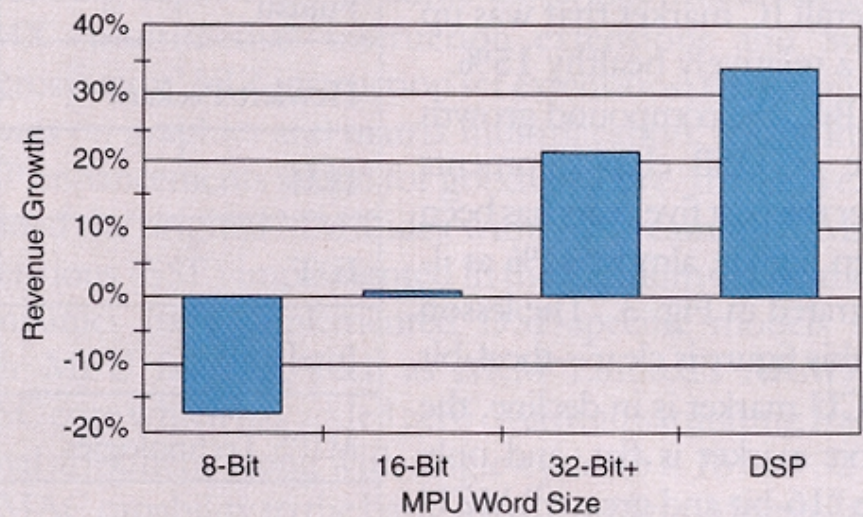
Company	Part	Key DSP Additions
Arm	ARM9E	Single-cycle integer MAC
Fujitsu	SPARClite family	Integer MAC and multimedia assist
Hewlett-Packard	PA-8000 family	Registers for MPEG decode
IBM	PowerPC family	Integer MAC
IDT	79RC4650 (MIPS)	Integer MAC
Intel	Pentium III	Streaming SIMD extensions
MIPS Technologies	MIPS64 5Kc	Single-cycle integer MAC
Motorola	PowerPC G4	Vector processor
Sun Microsystems	UltraSPARC family	VIZ Imaging Instruction Set

Market Growth of DSP/MCU/MPU

Five-Year MCU Market Growth versus DSP



Five-Year MPU Market Growth versus DSP



Conclusions

- Embedded Processor will be the key issues for product development
- Application domain specific architecture will dominate either in MPU or DSP for embedded systems
- IP core based design will be the solution of the time to market and time to benefit
- QoS plays the role the success